# CAeSaR: unified Cluster-Assignment Scheduling and communication Reuse for clustered VLIW processors

Vasileios Porpodas [†] and Marcelo Cintra [†⋆]

School of Informatics, University of Edinburgh[†]
Intel Labs Braunschweig[⋆]

CASES 2013

# Energy efficiency, VLIWs and Scheduling

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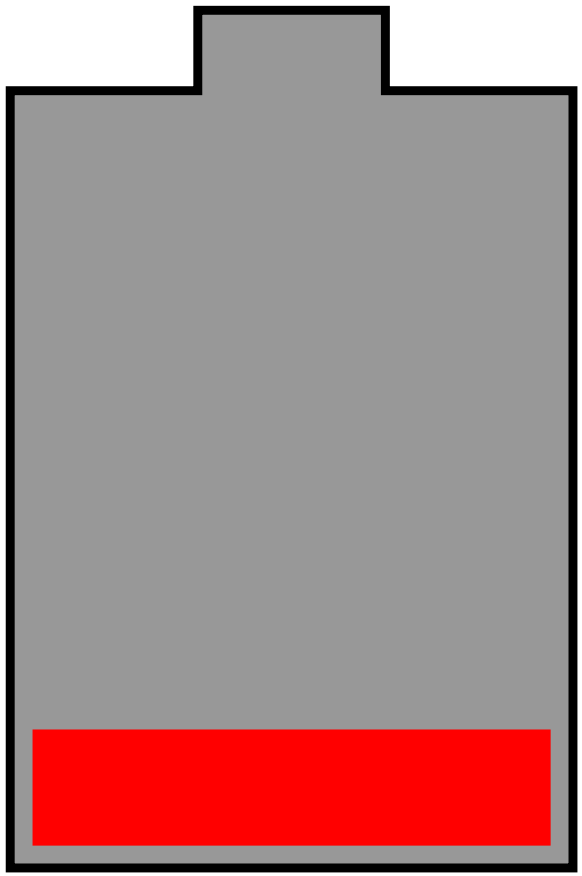

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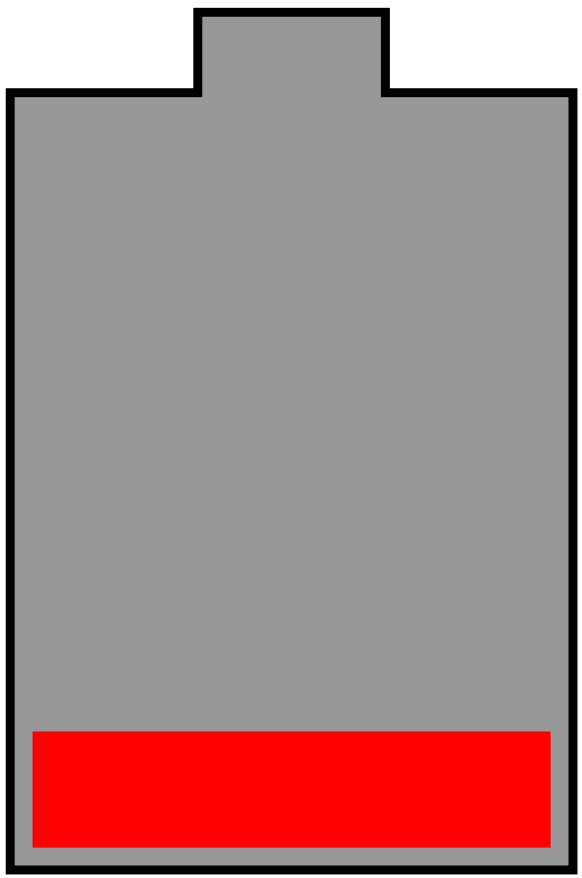

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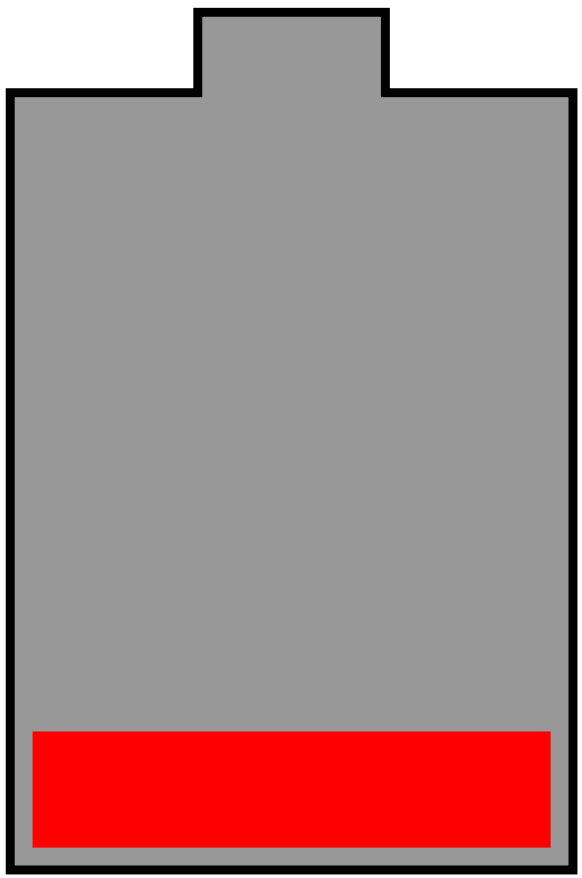

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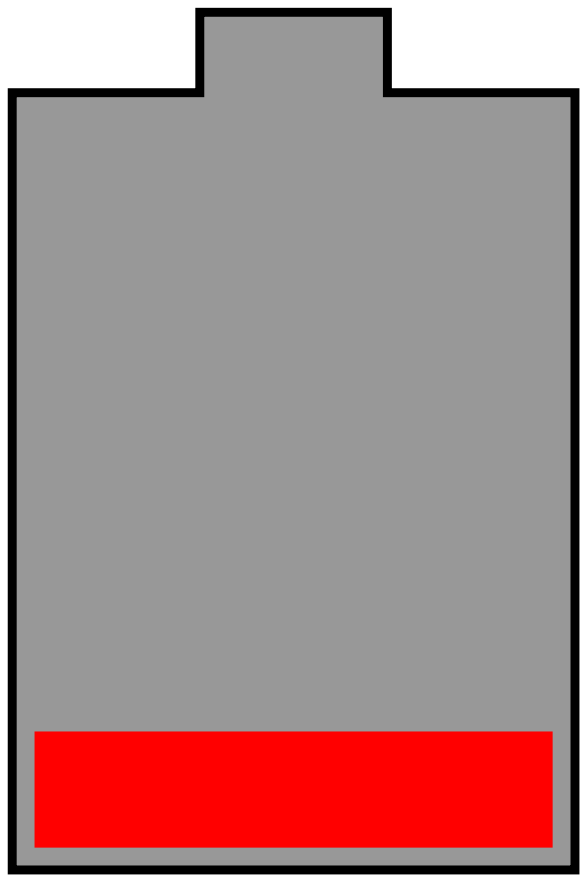
- Clustered VLIW = scalable VLIW.



# Clustered VLIW

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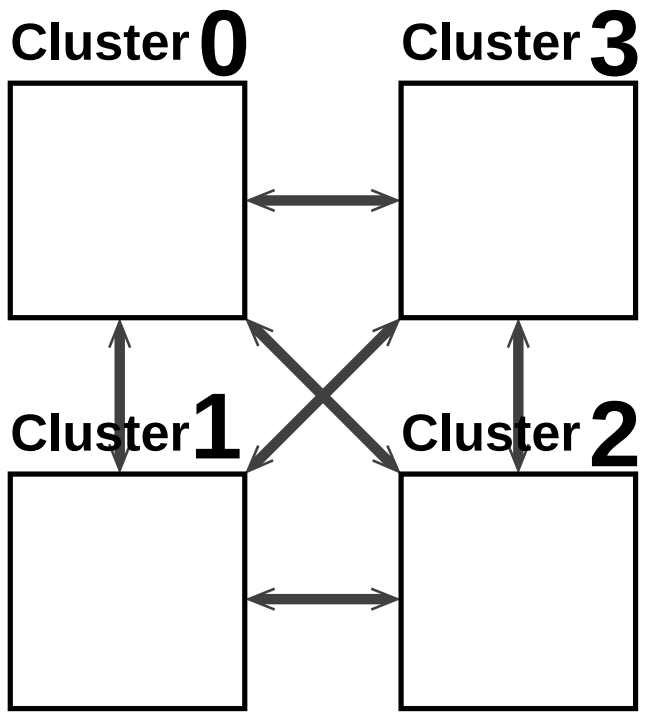

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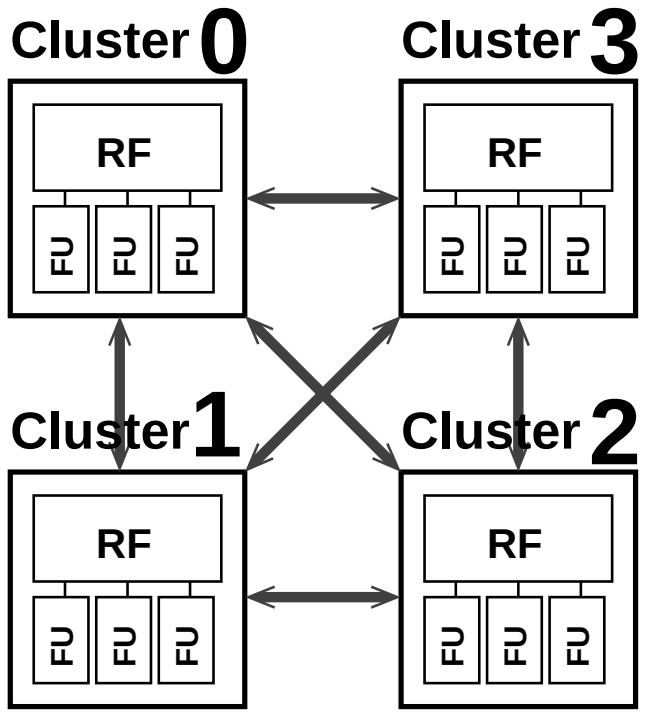
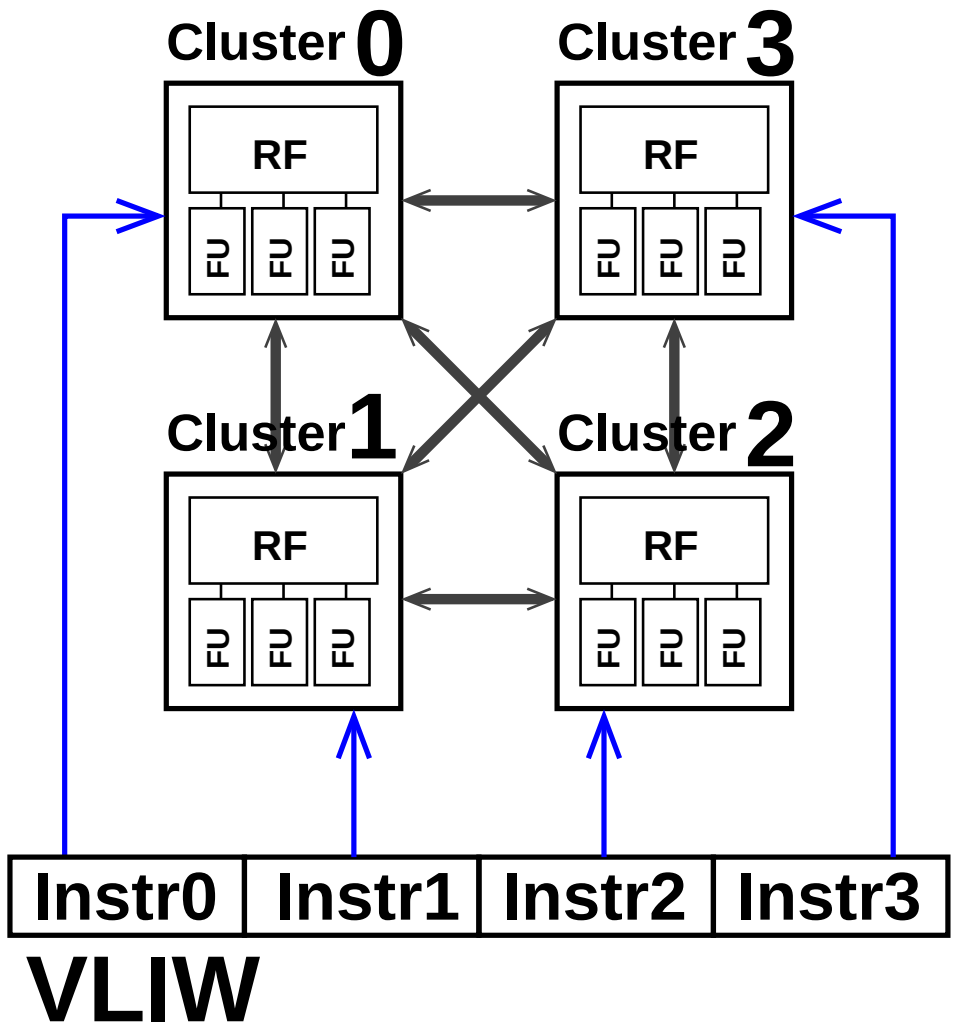


# Clustered VLIW

- Scalable
- Energy efficient
- High frequency
- Inter-Cluster delay
- Relies on compiler
- Statically scheduled
- Explicit ILP



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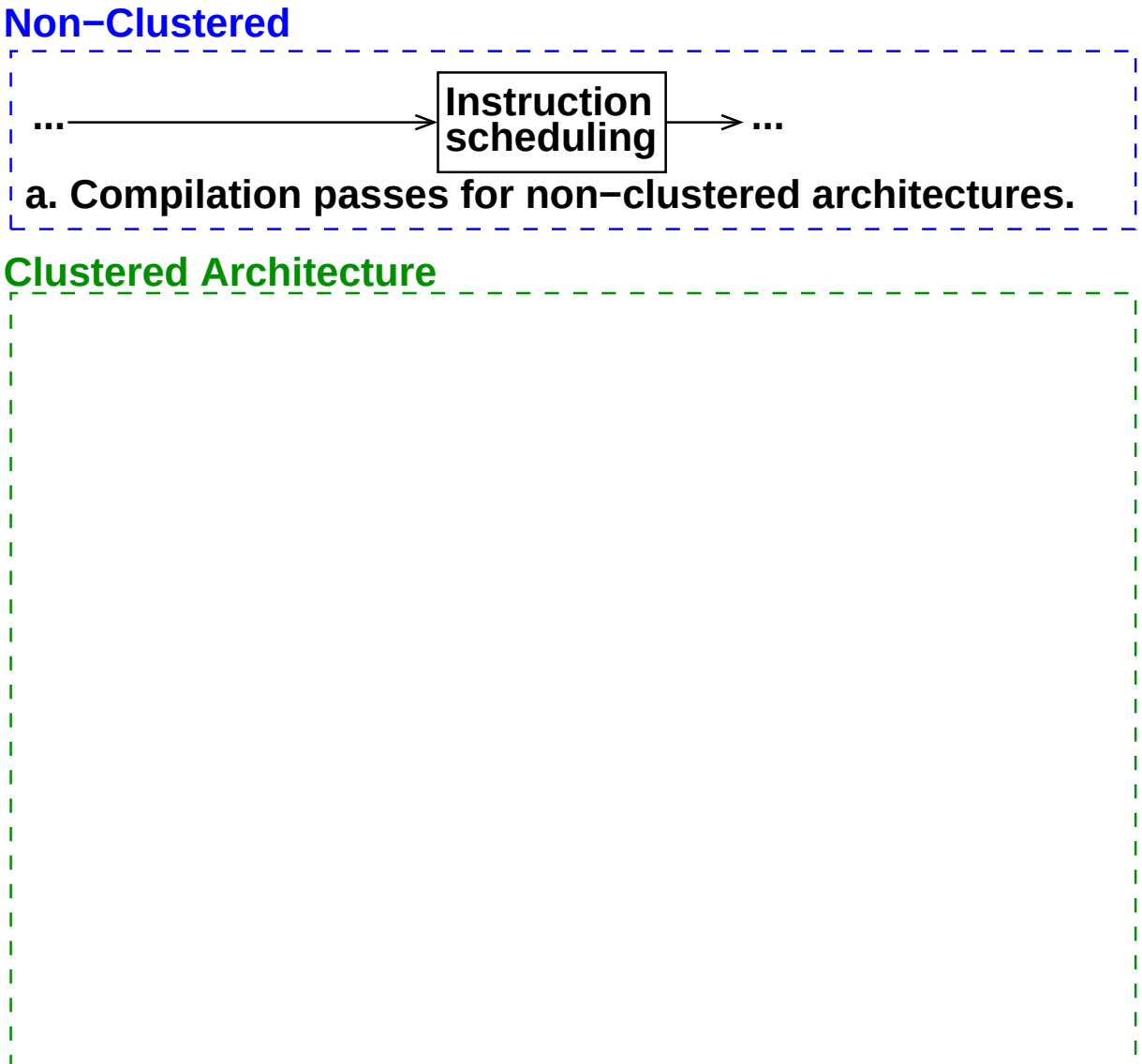

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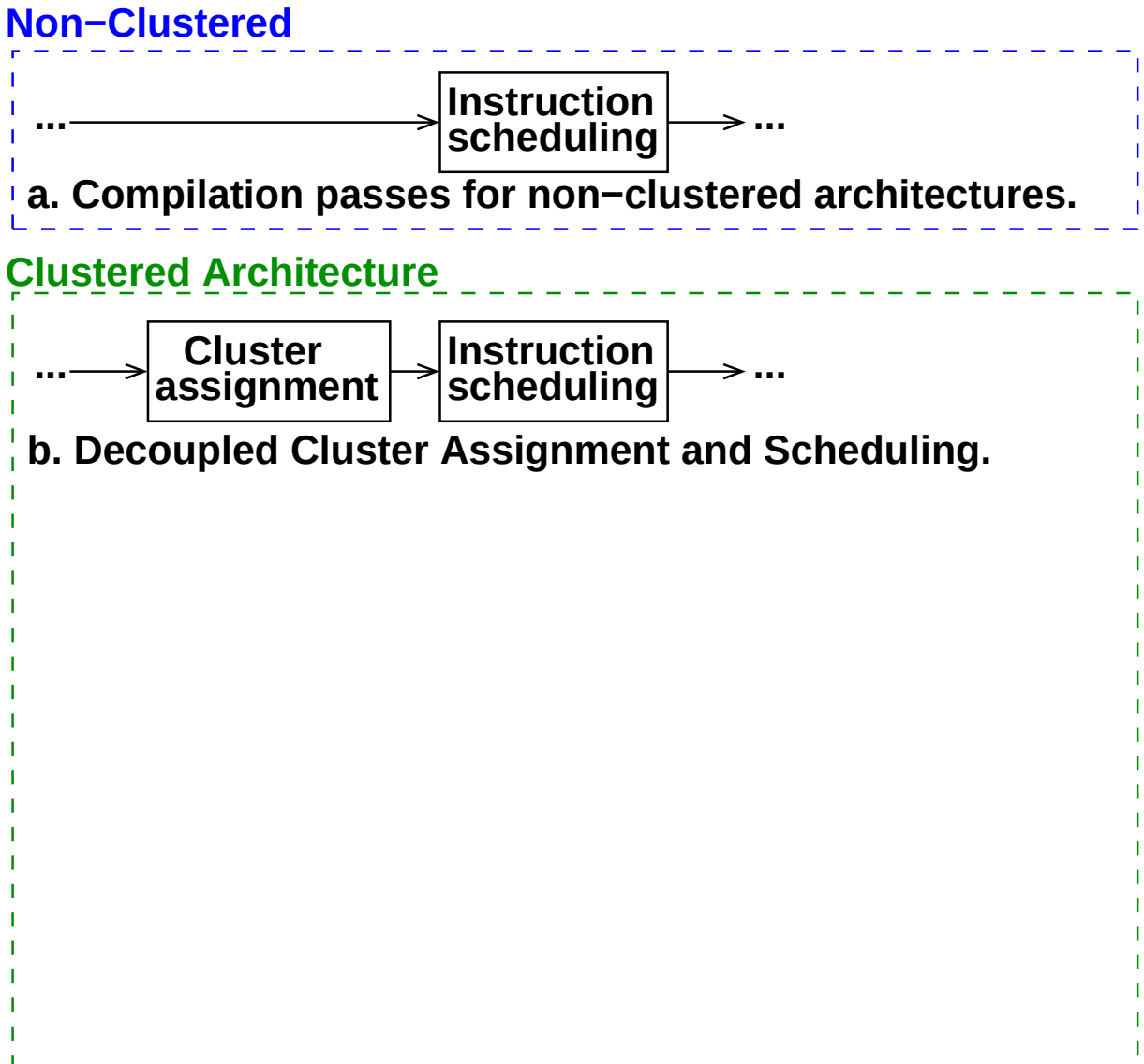

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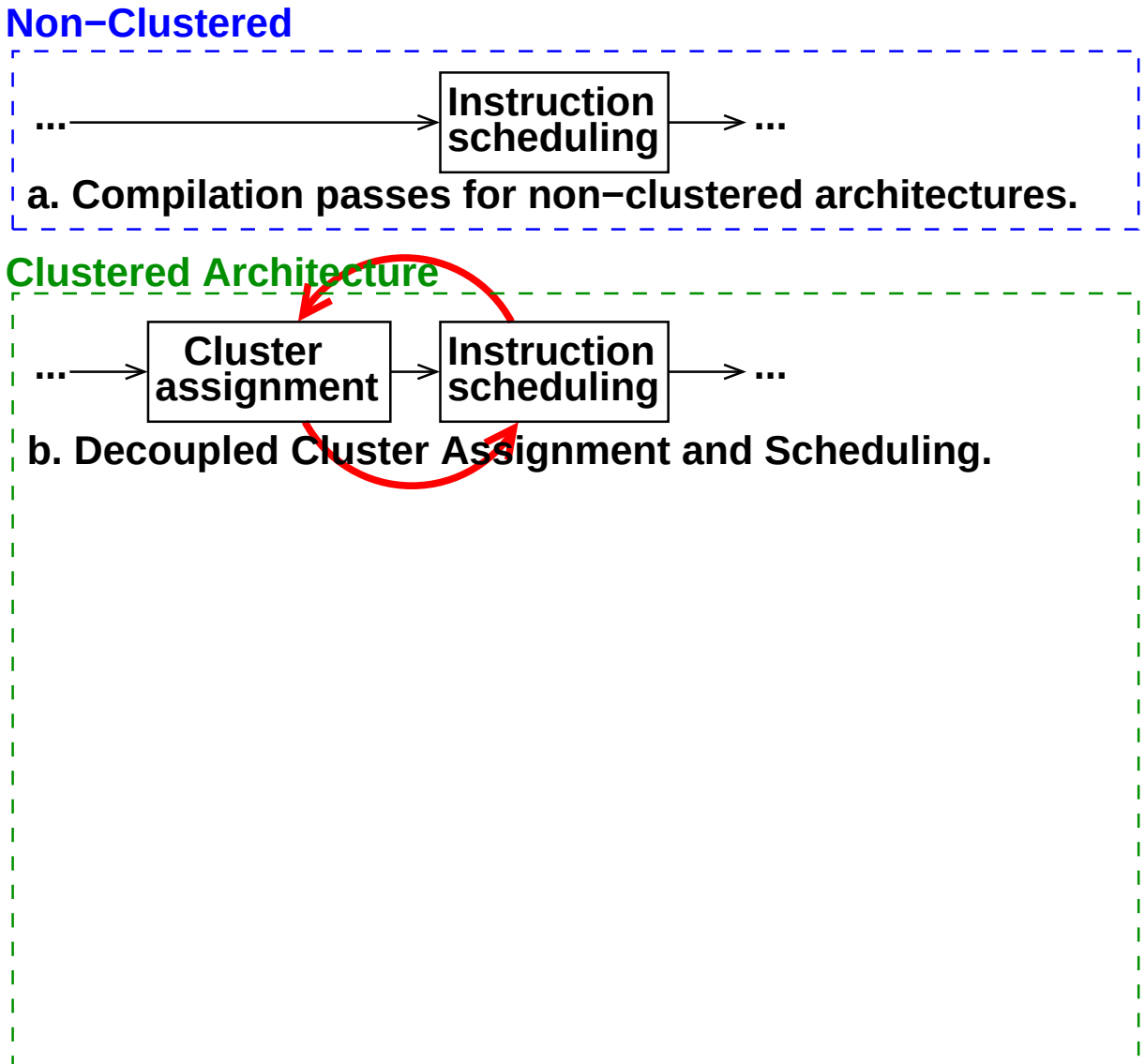

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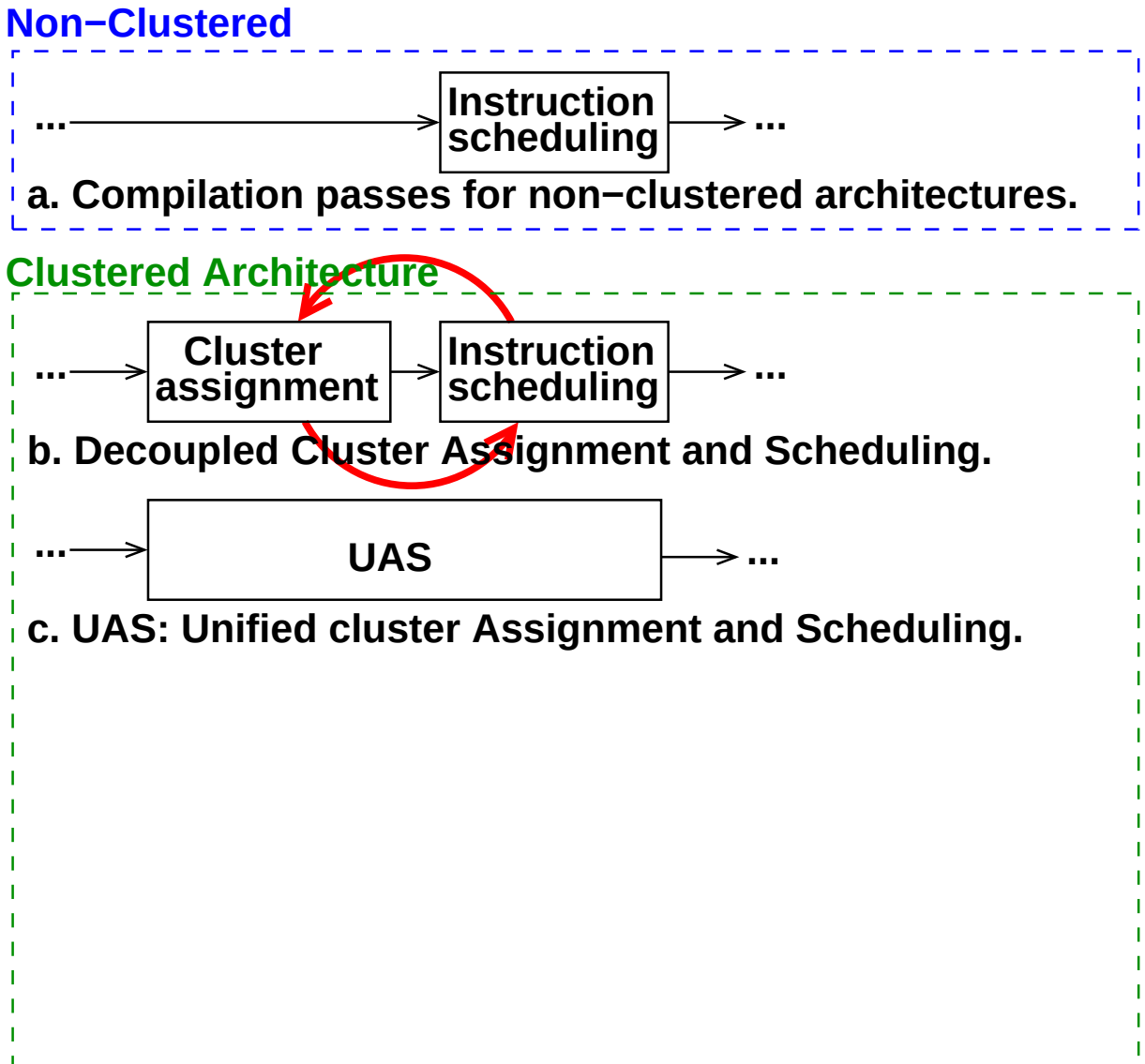

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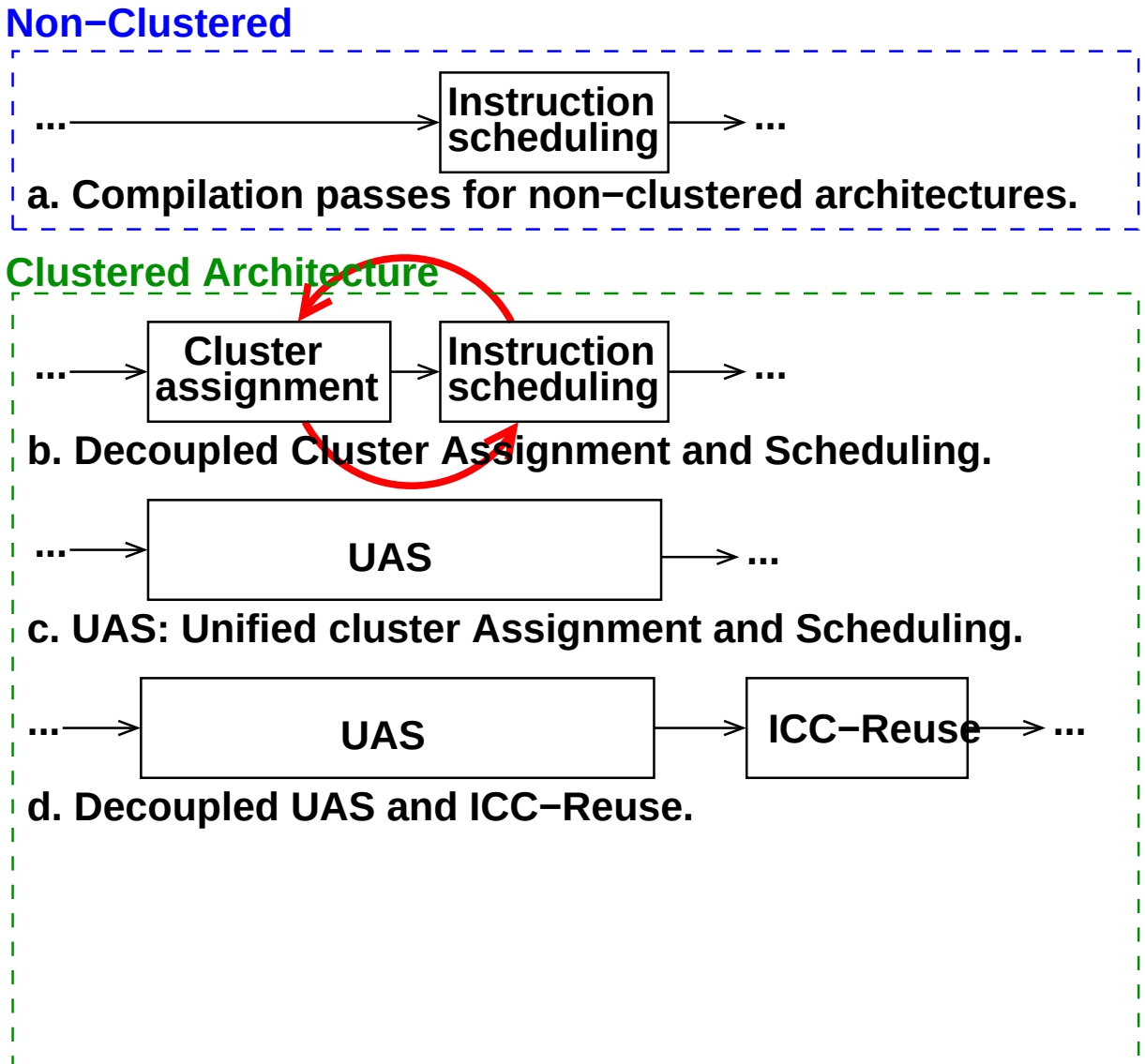

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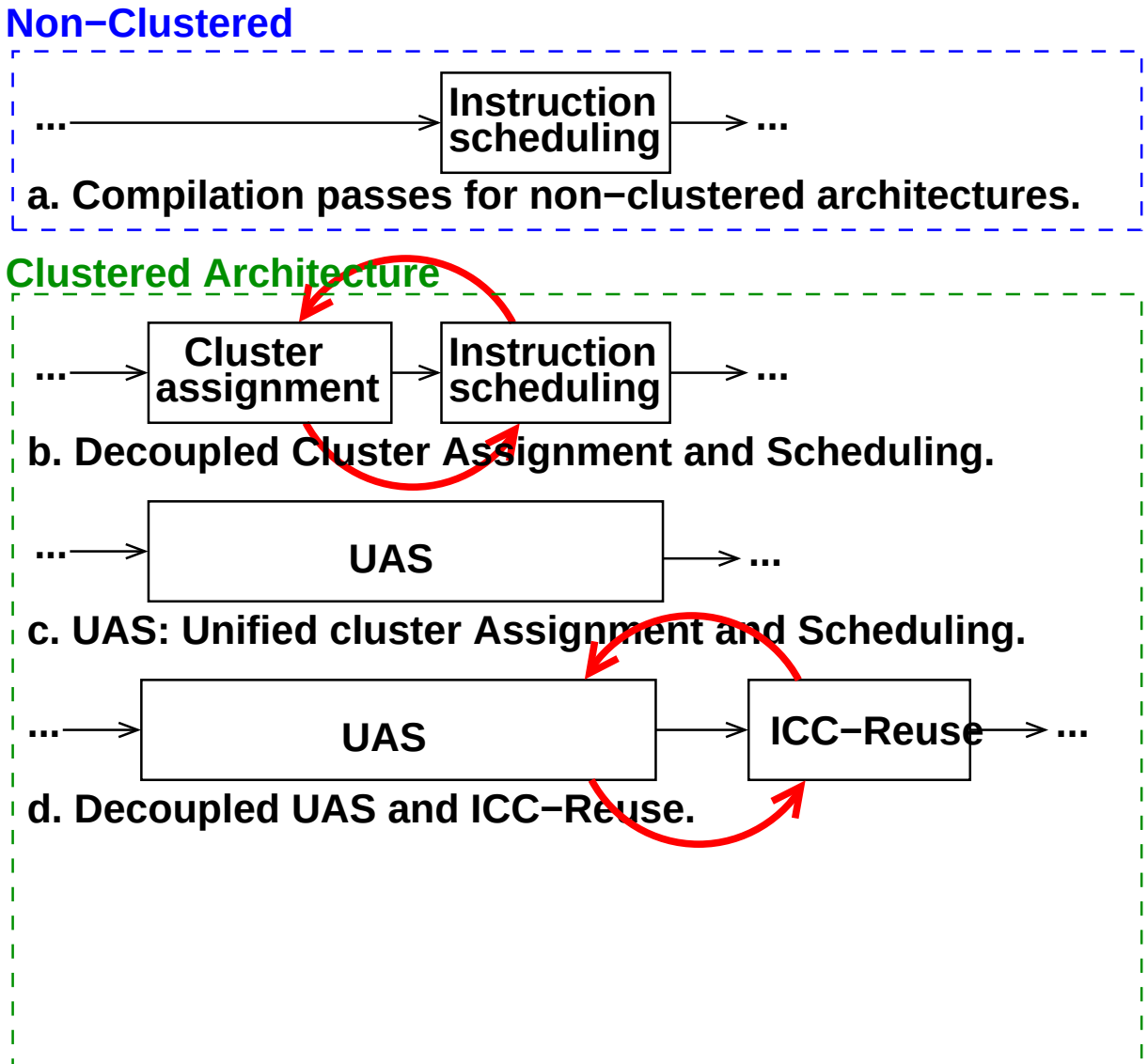

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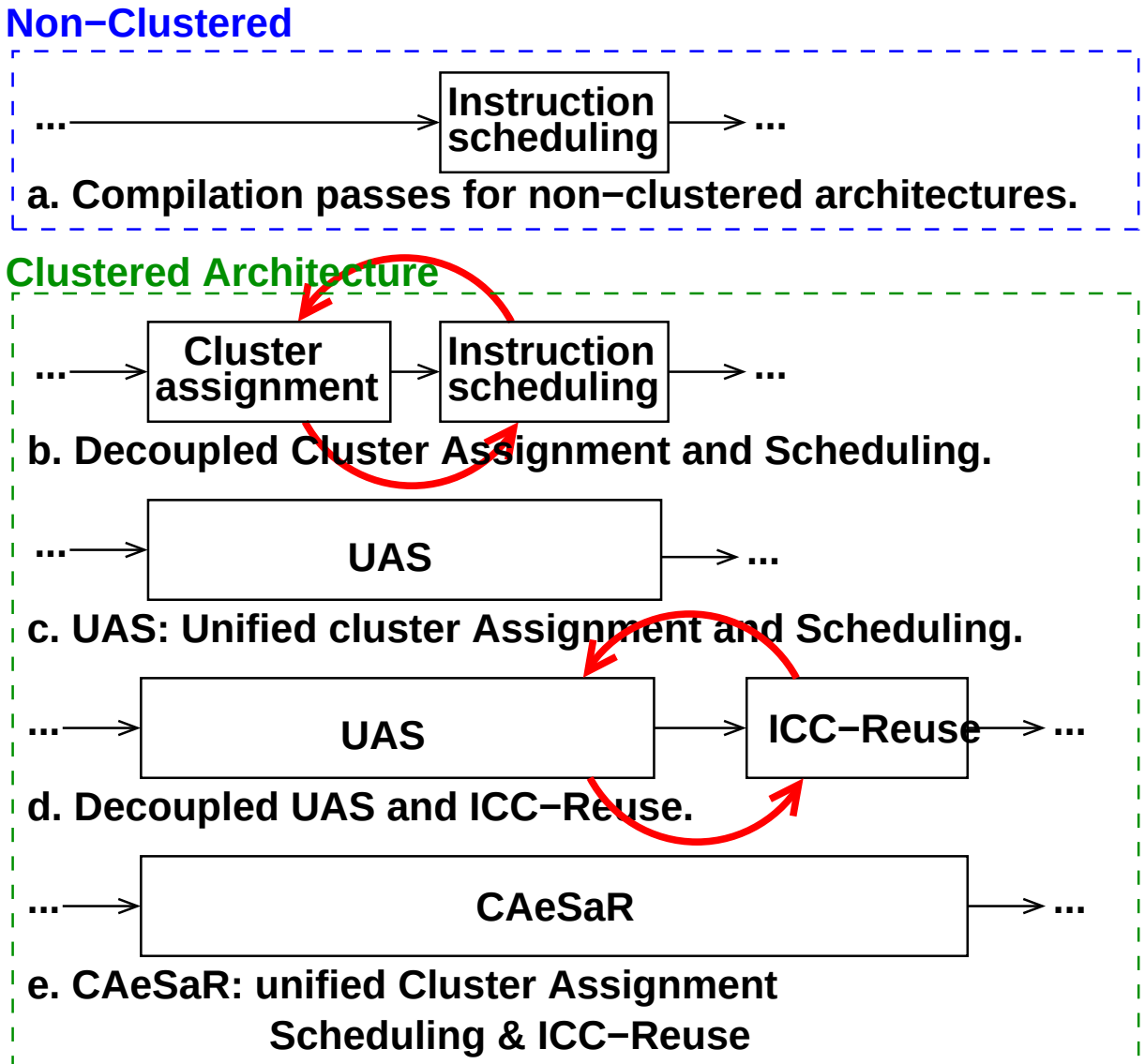

# Outline

Introduction

CAeSaR Scheduling

Experimental Setup and Results

Conclusion

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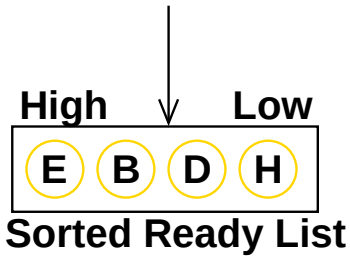


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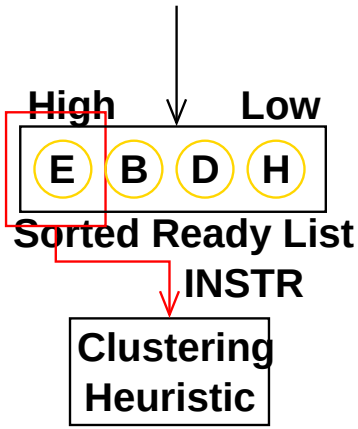

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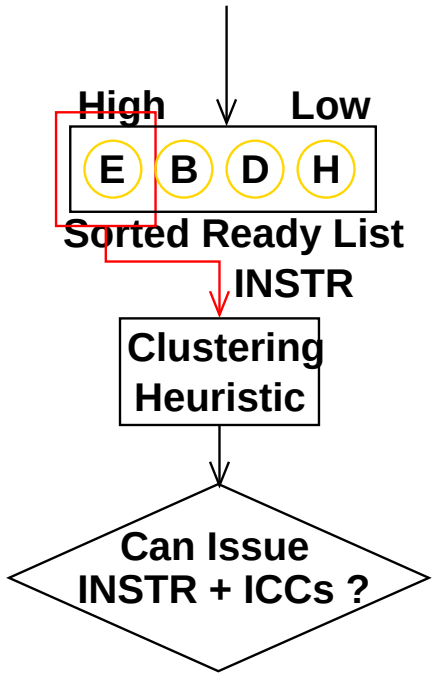

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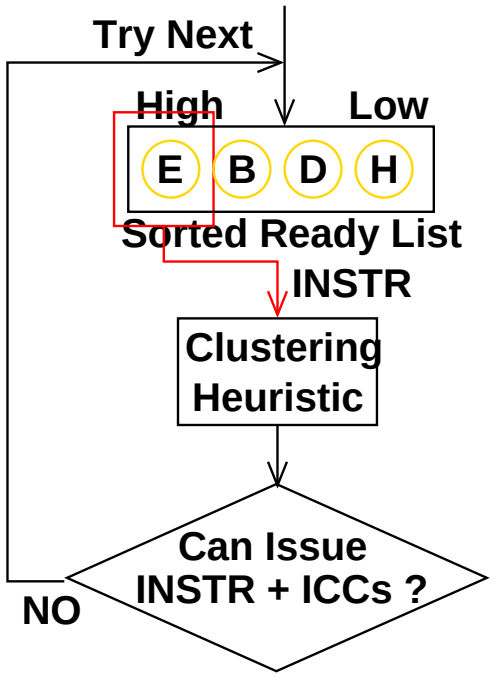

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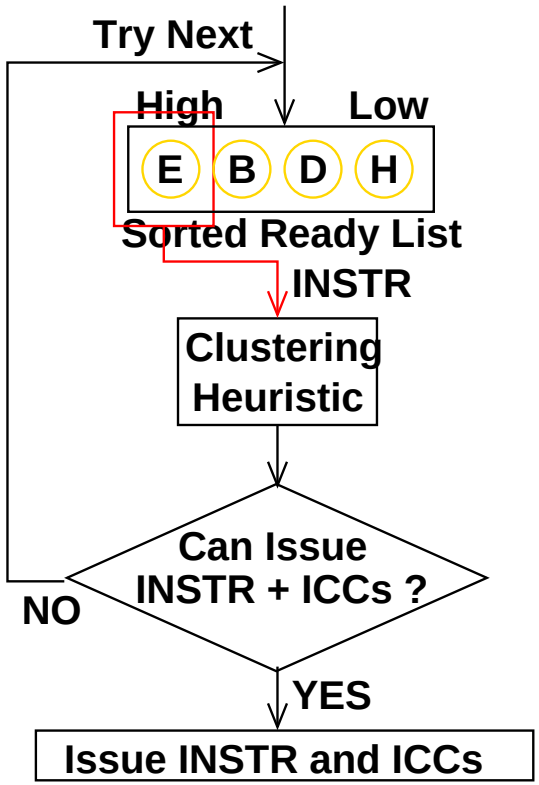

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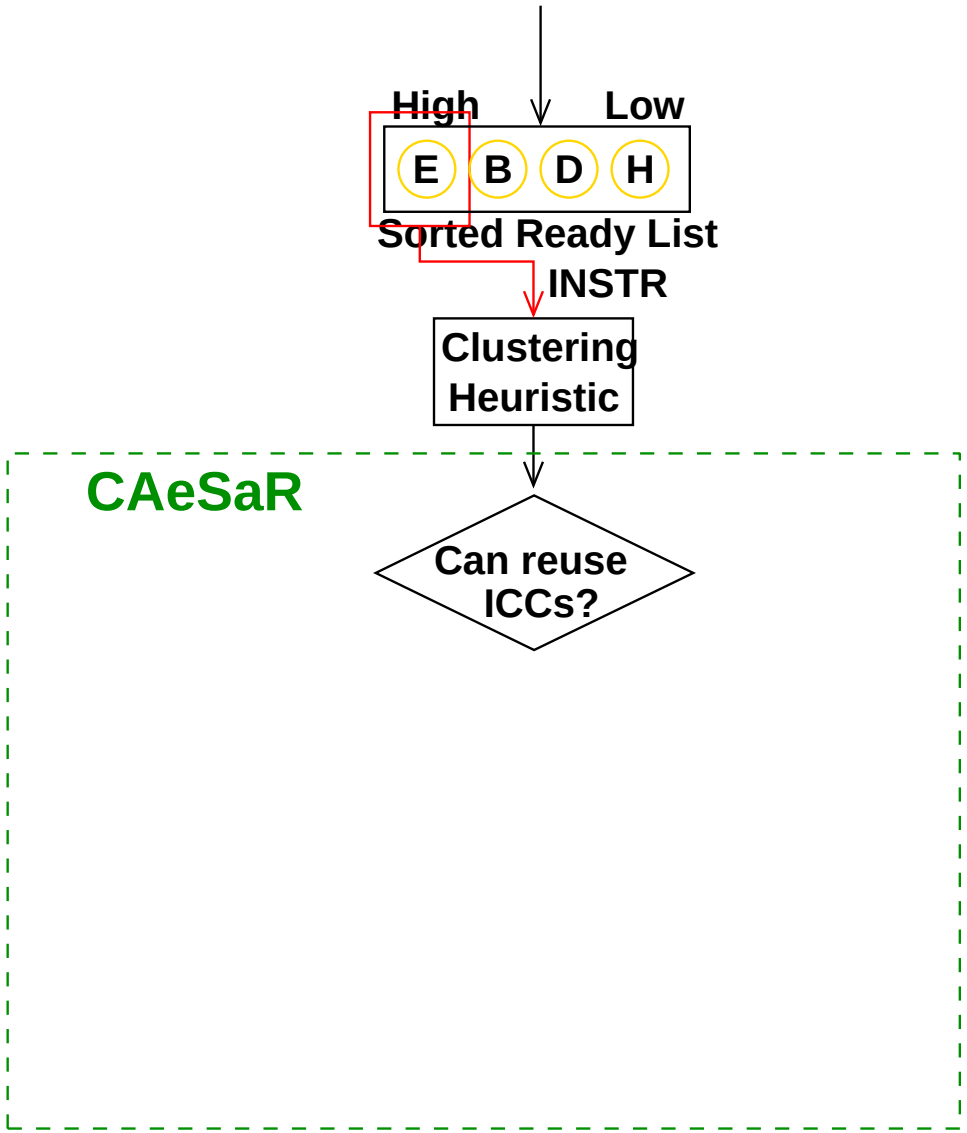

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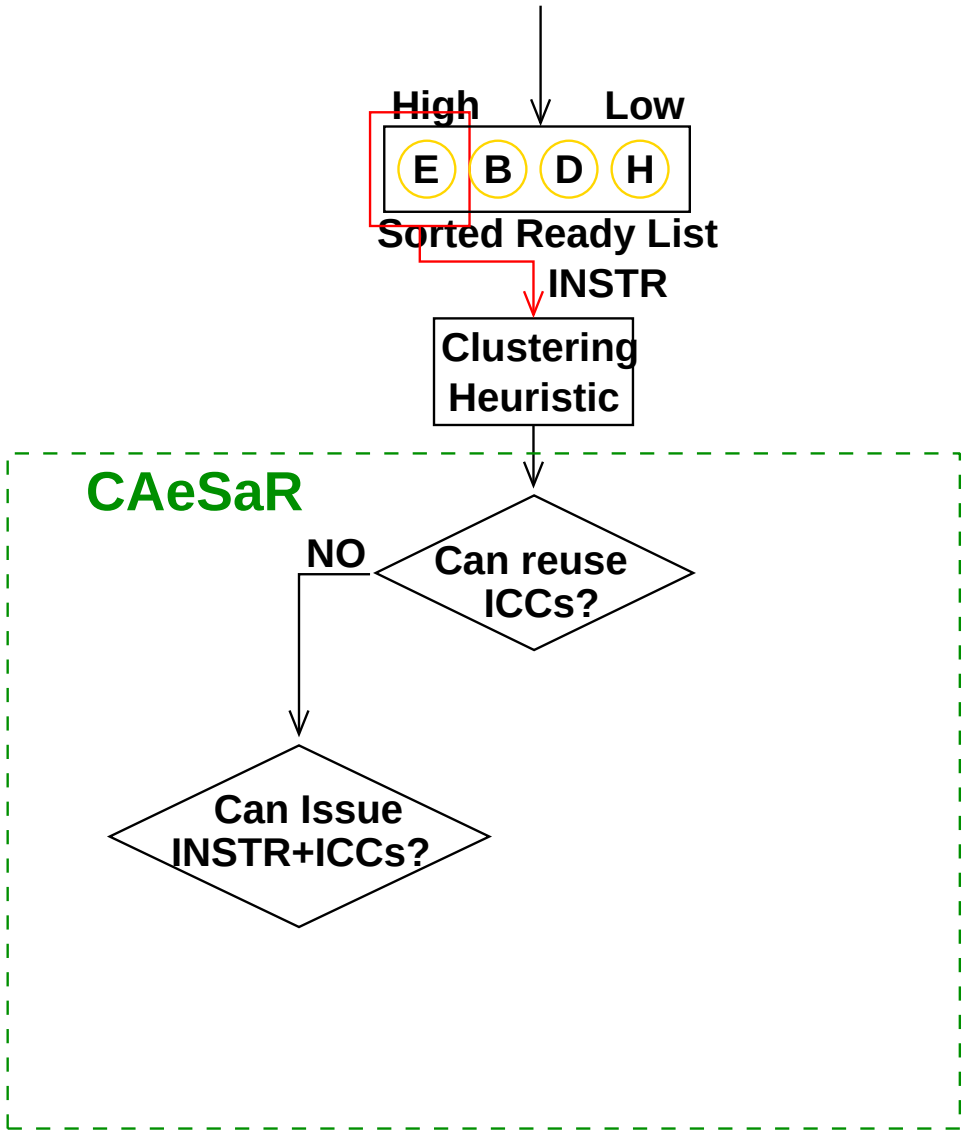

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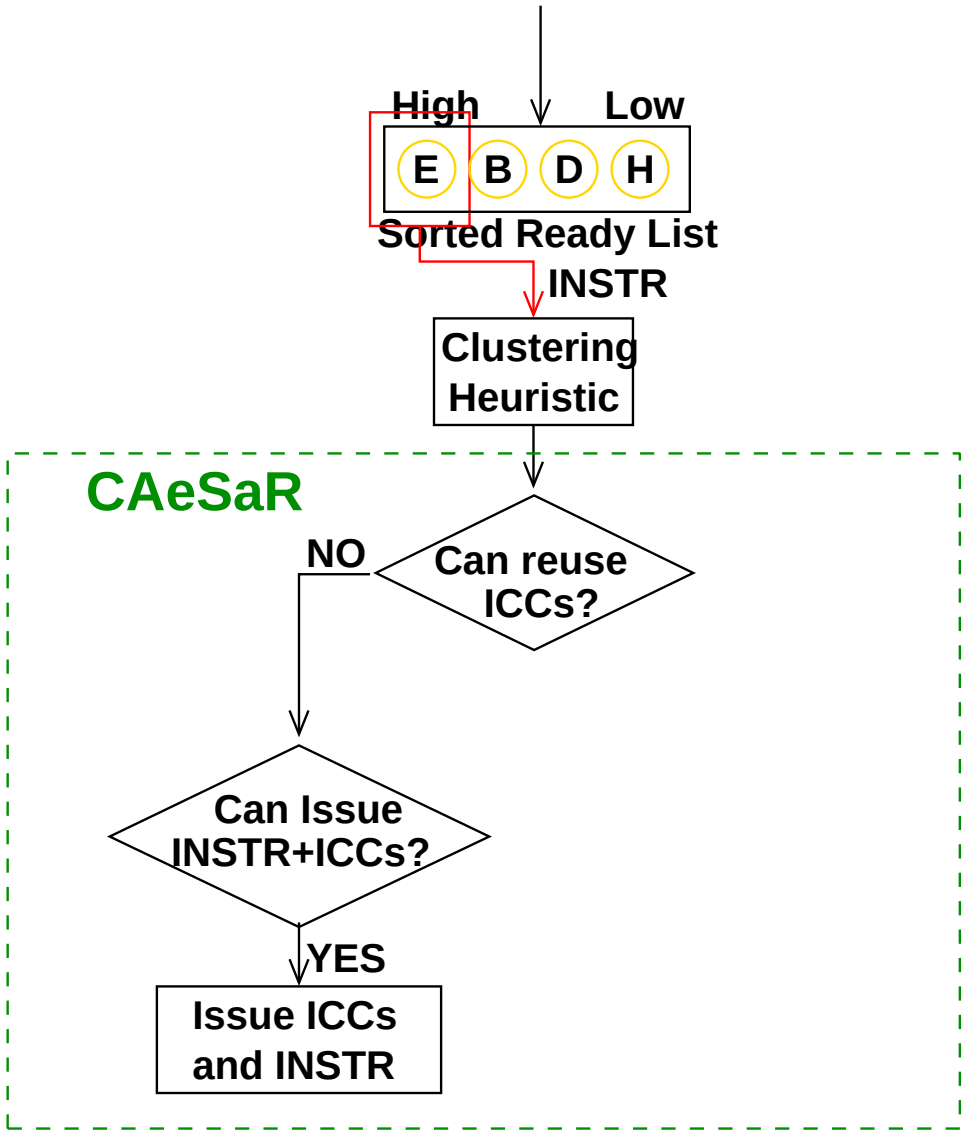

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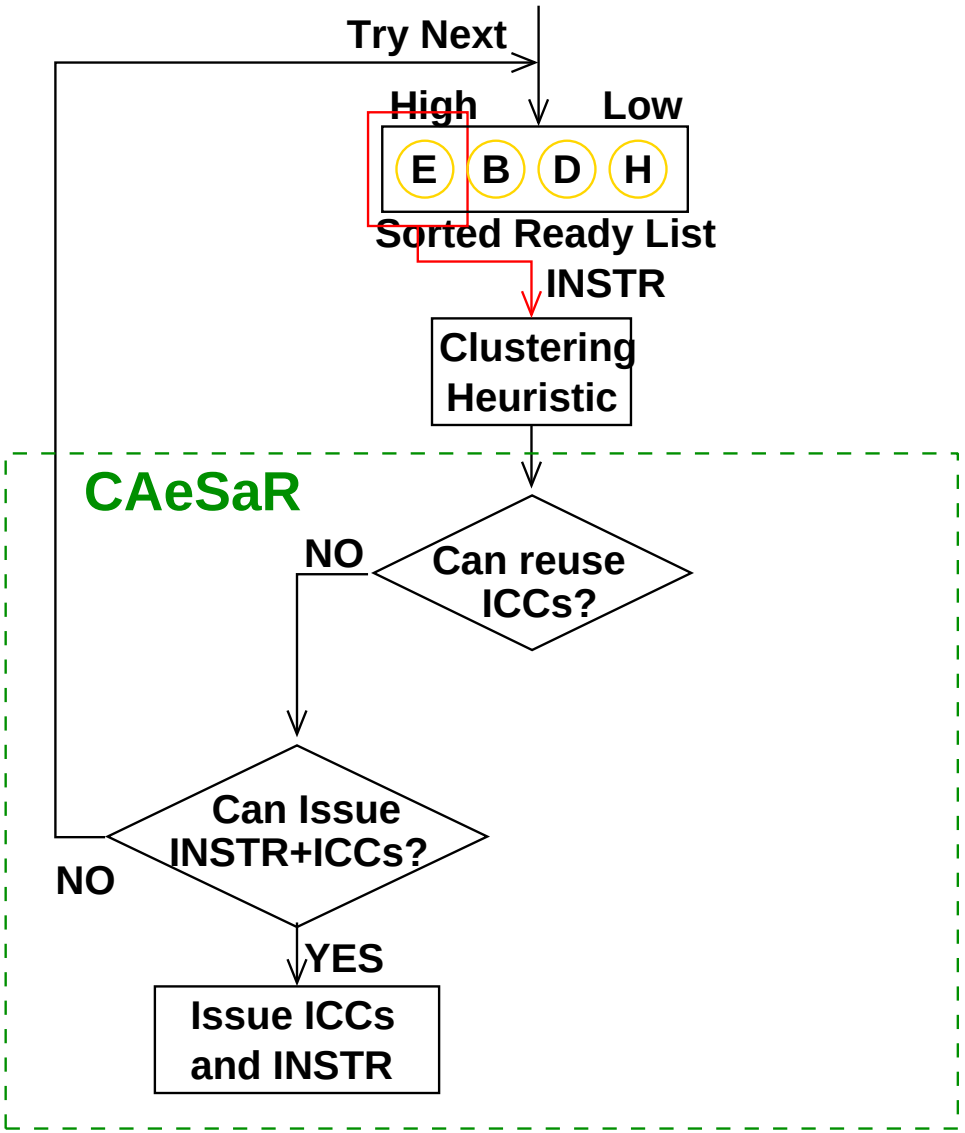

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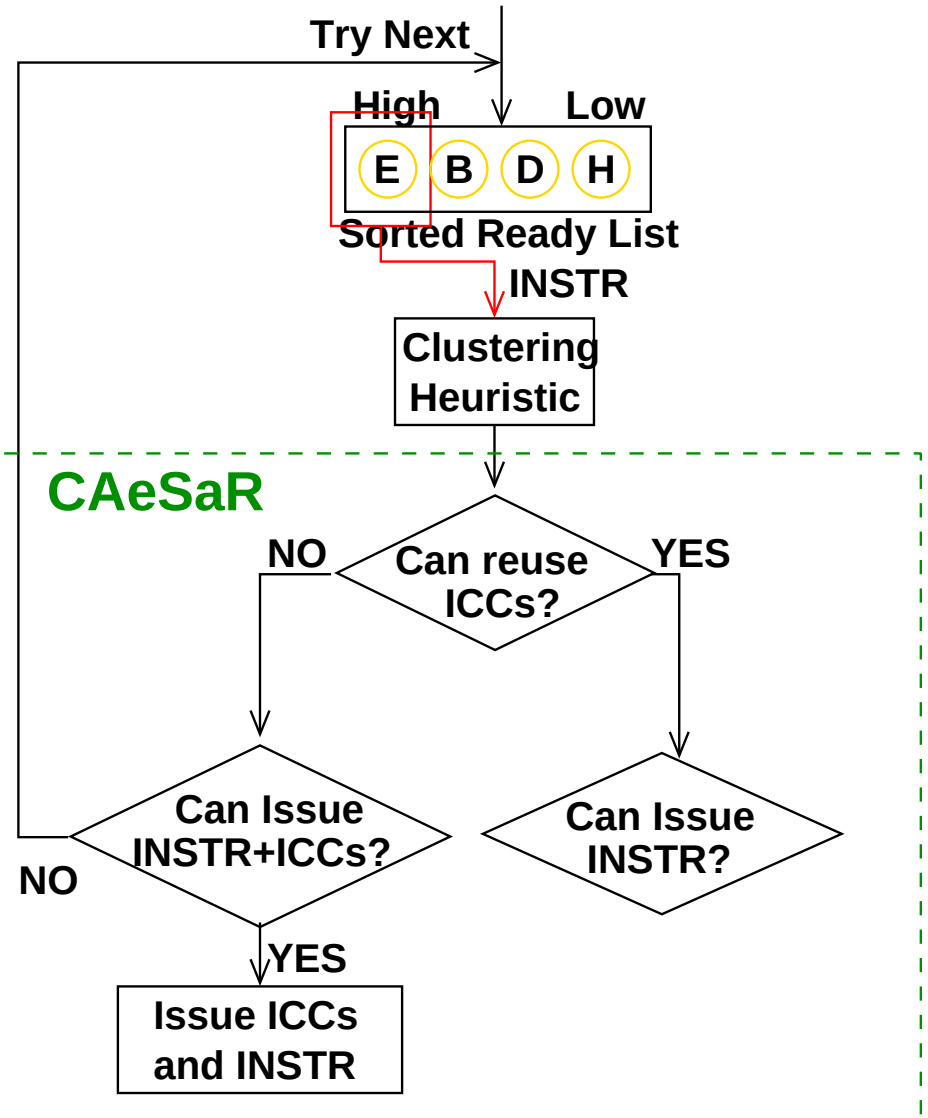

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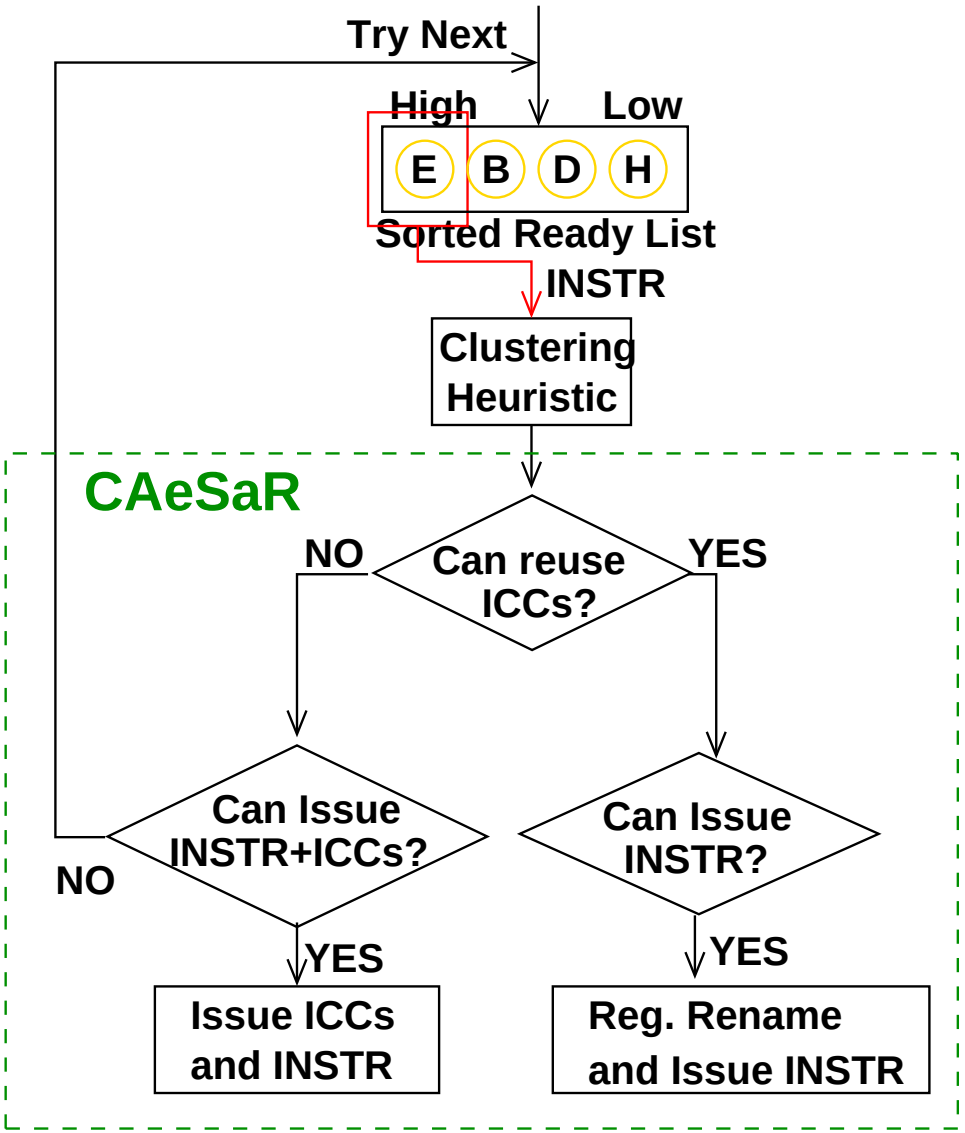

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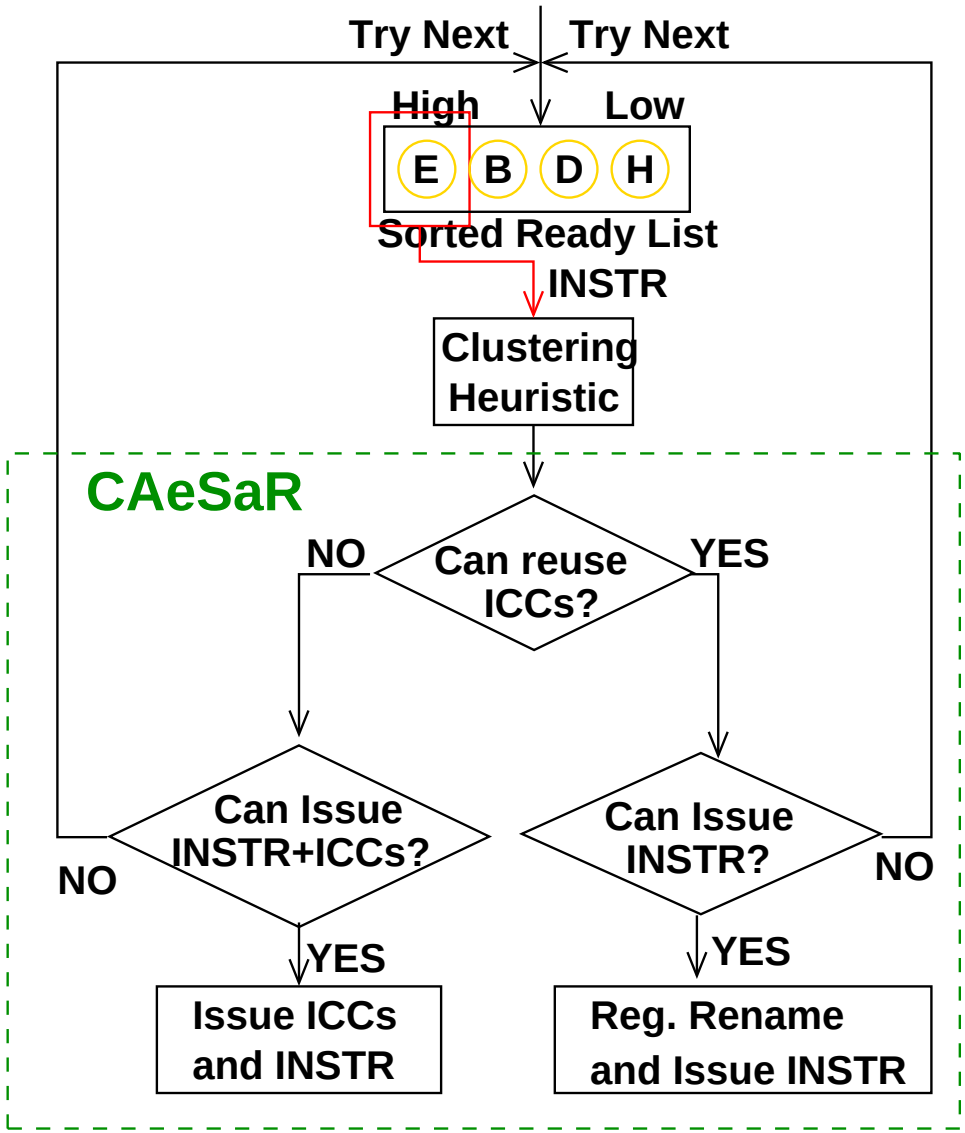


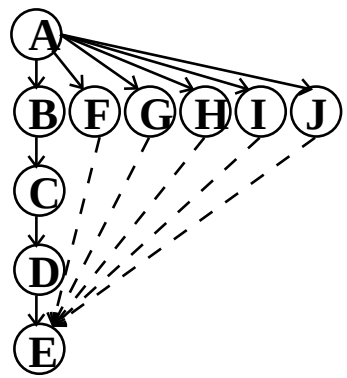
# Example

**Monolithic**

| | | |
|---|---|---|
| 0 | A | |
| 1 | B | F |
| 2 | C | G |
| 3 | D | H |
| 4 | I | J |
| 5 | E | |

**a. VLIW**

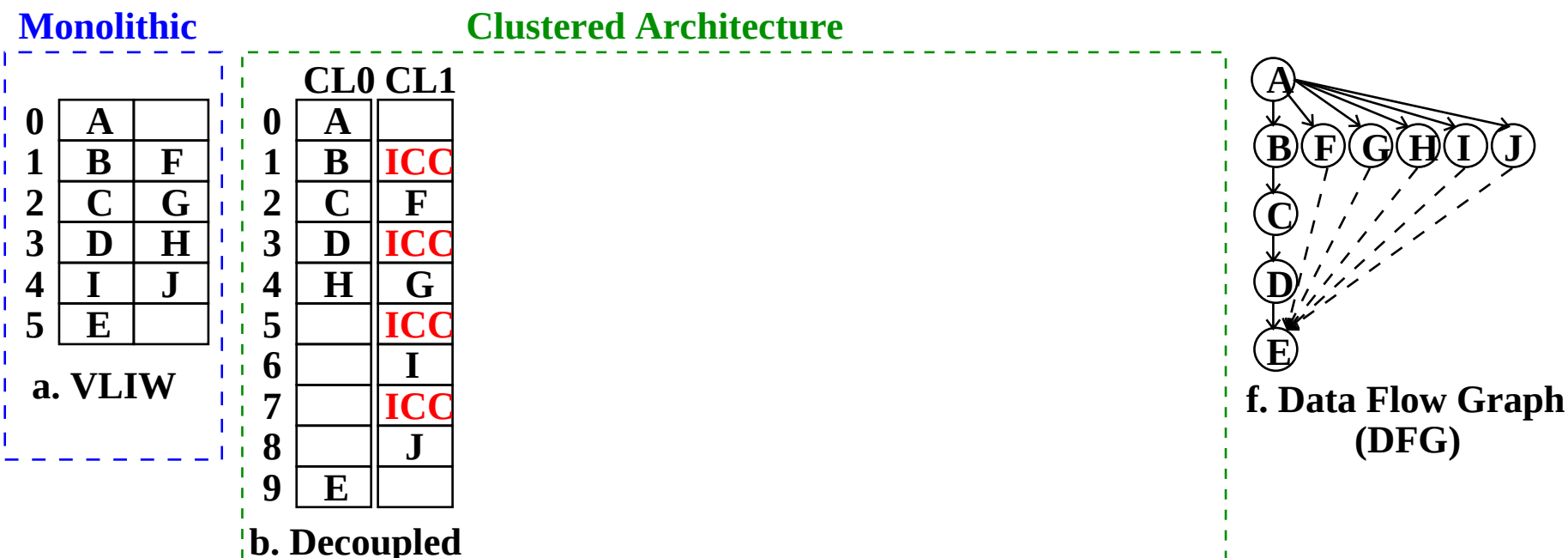
**Clustered Architecture**




**f. Data Flow Graph (DFG)**

# Example

- 2-step scheduler generates bad schedule



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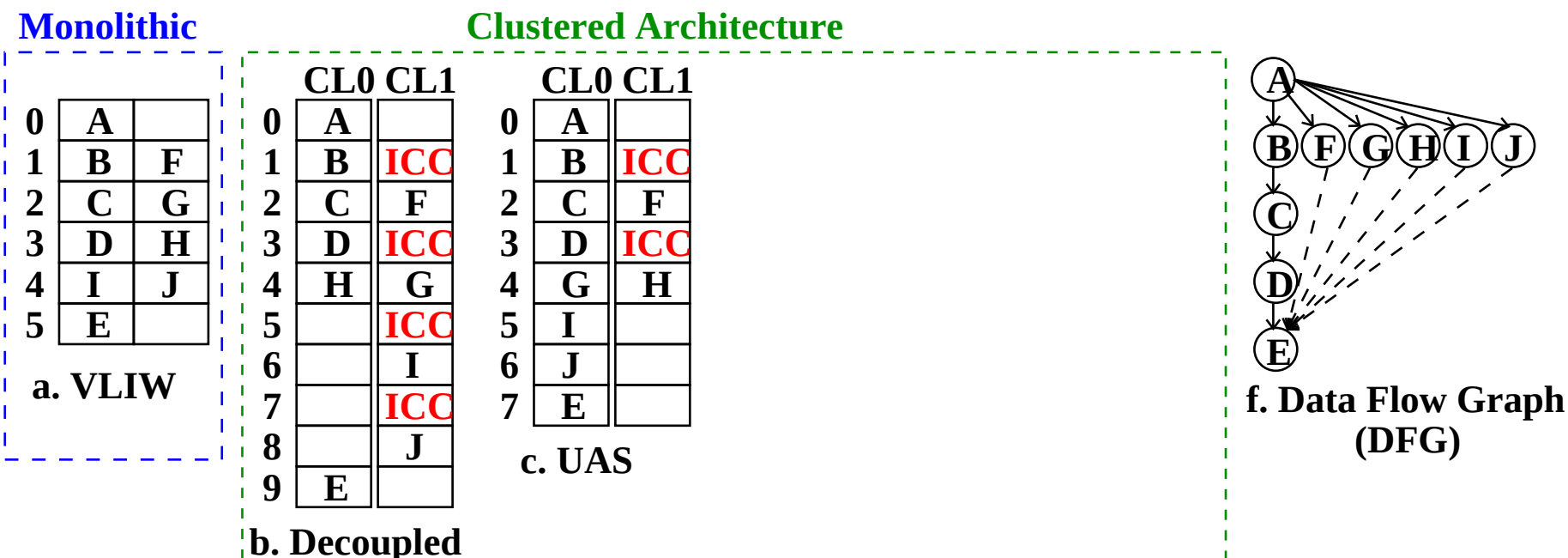

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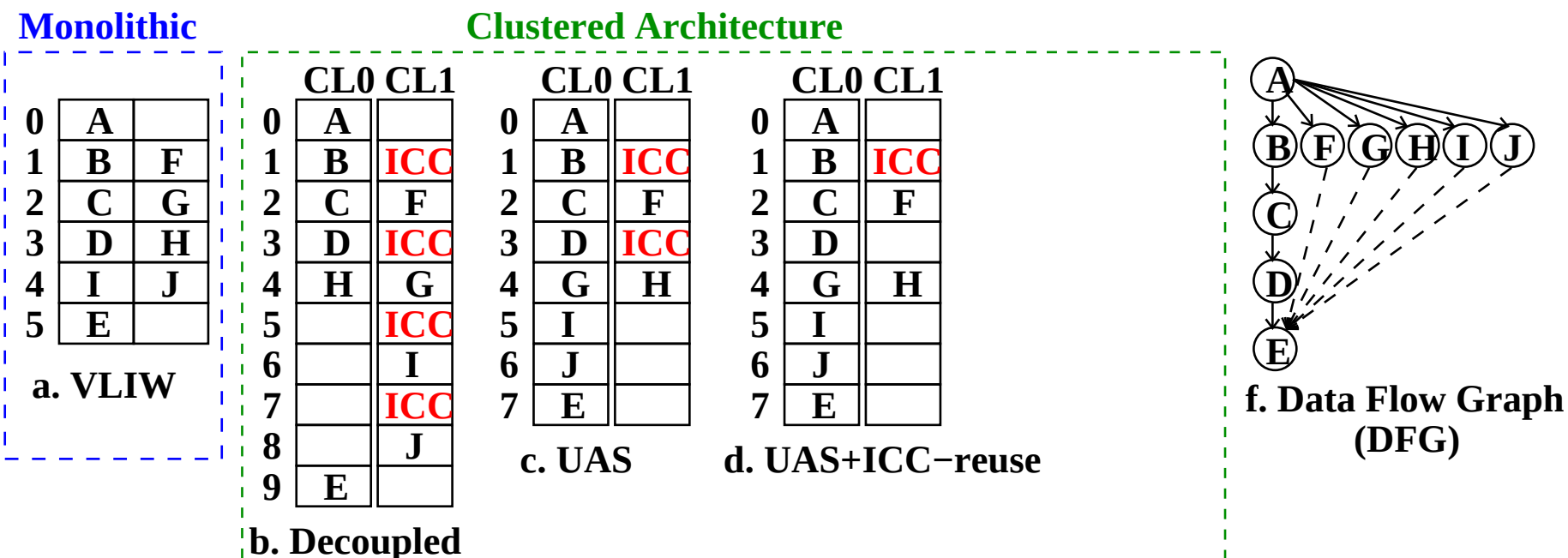

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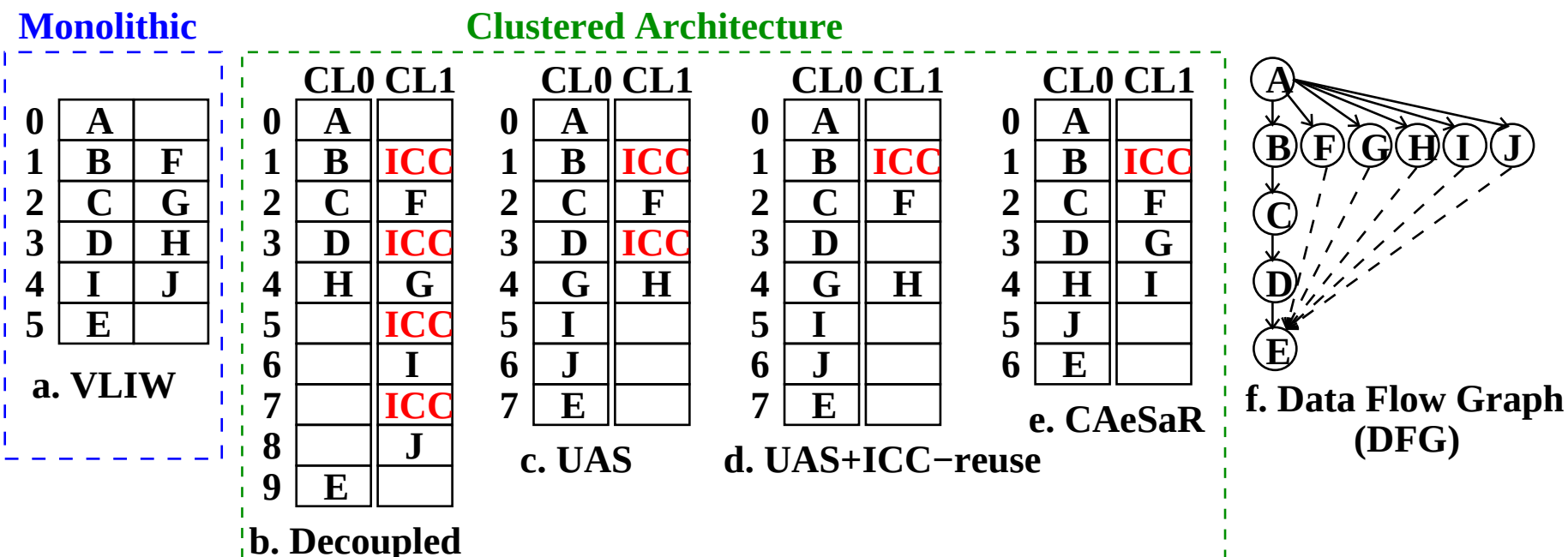

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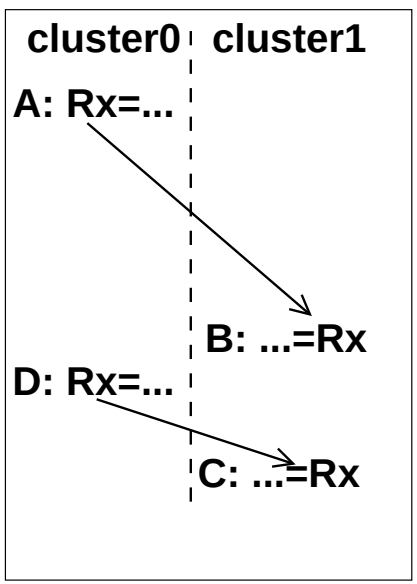


a. Before ICCs

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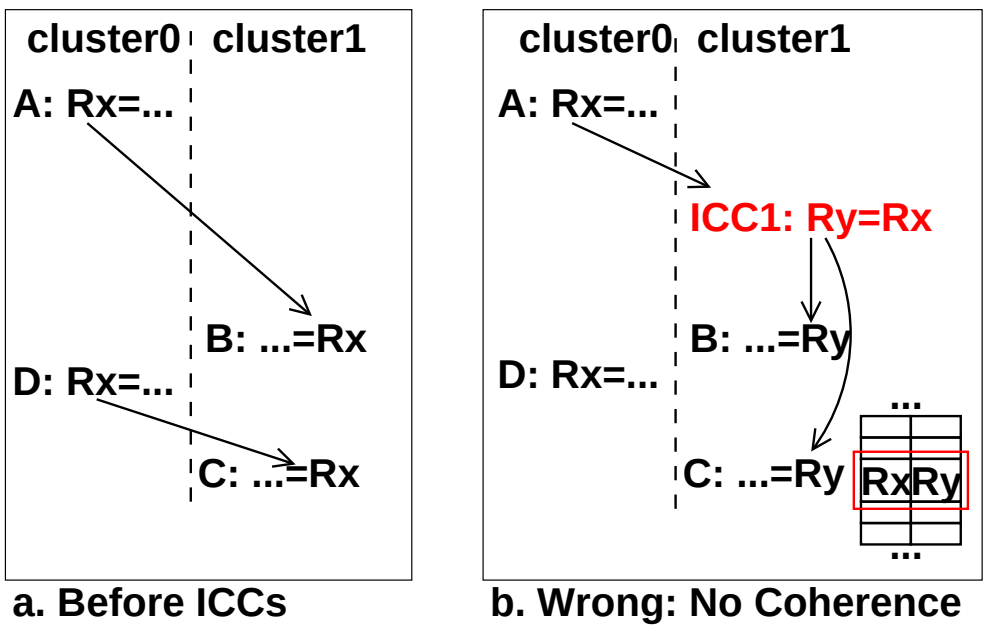

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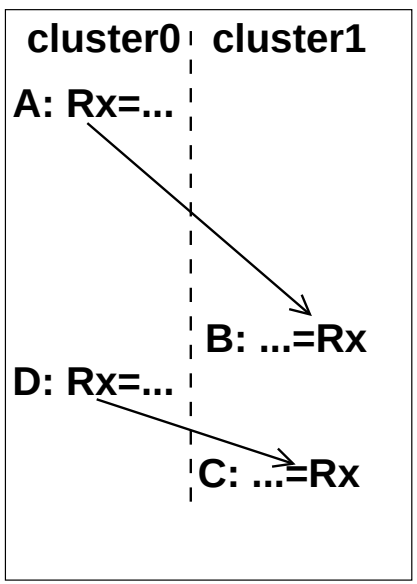


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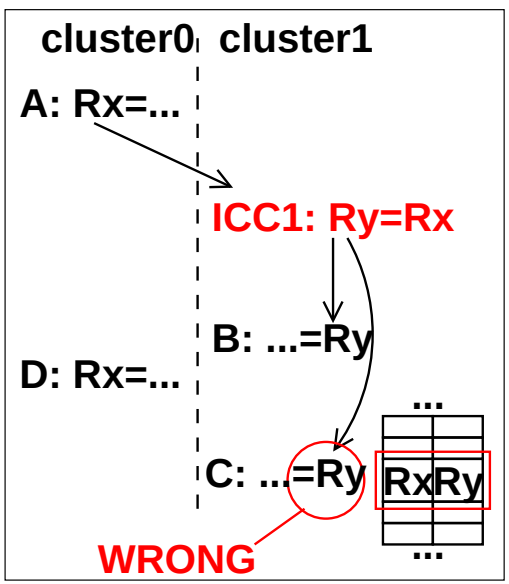


b. Wrong: No Coherence

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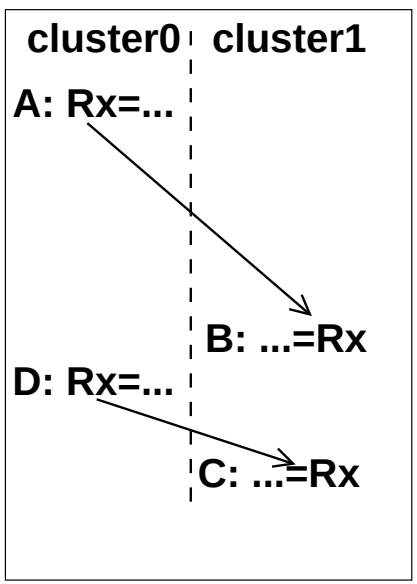
- CAeSaR follows an approach similar to write-invalidate cache coherent protocols

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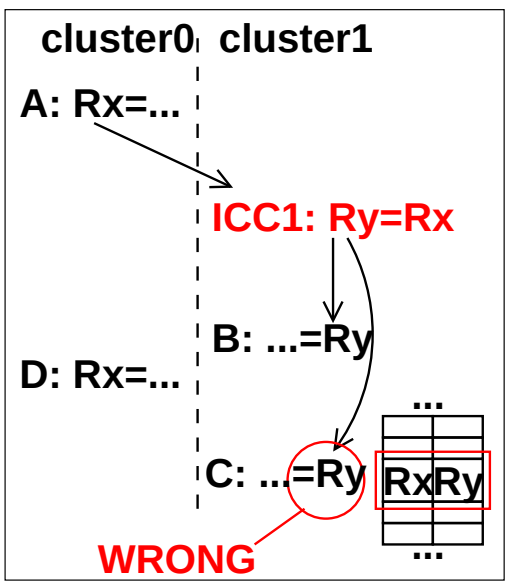


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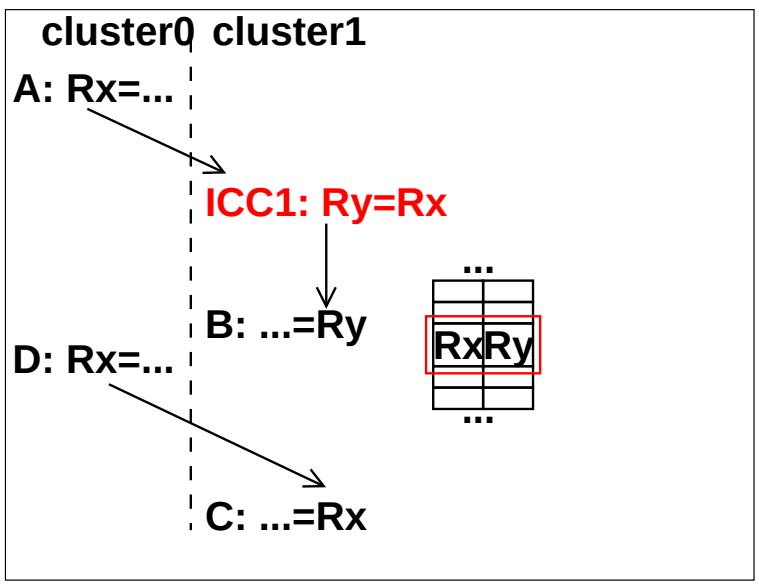


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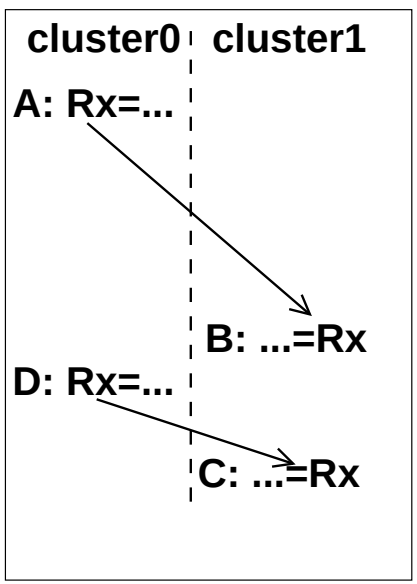


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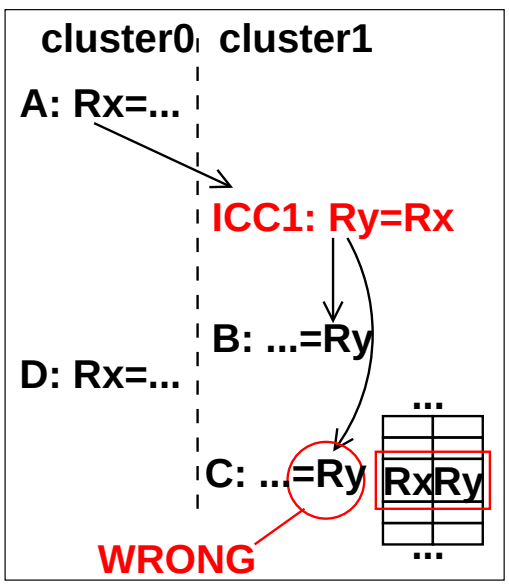


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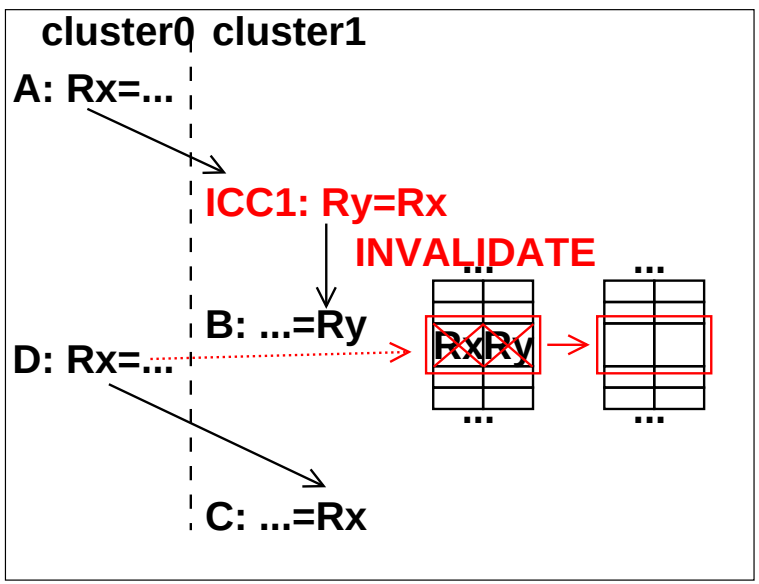


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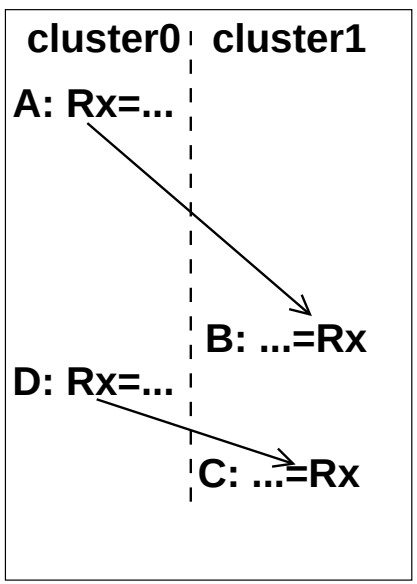


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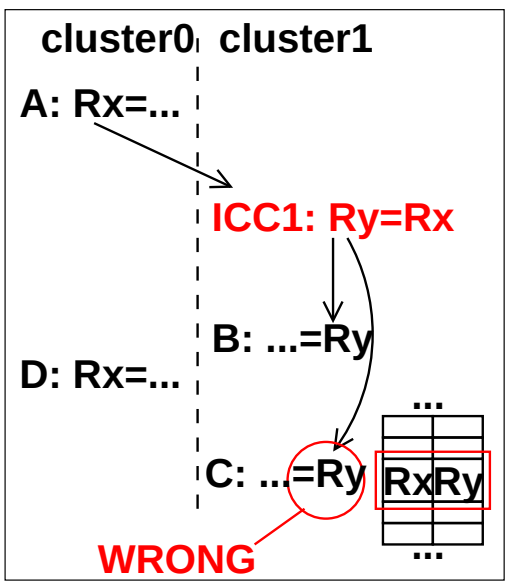


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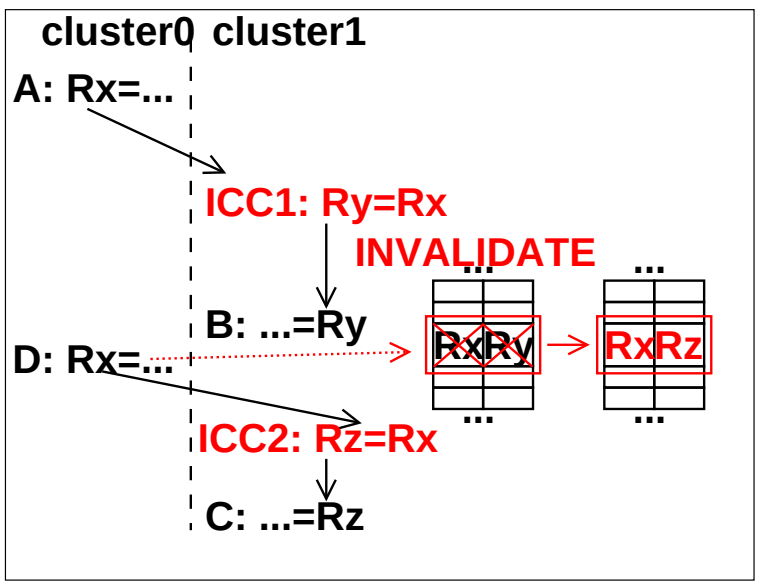


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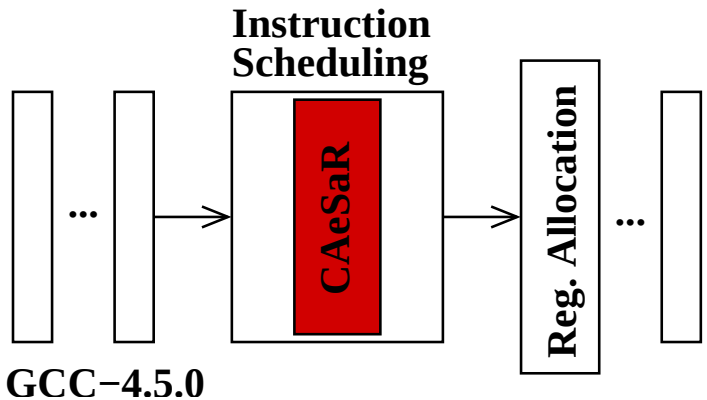
# Experimental Setup

- Compiler: GCC-4.5.0, Modified Haifa-Scheduler



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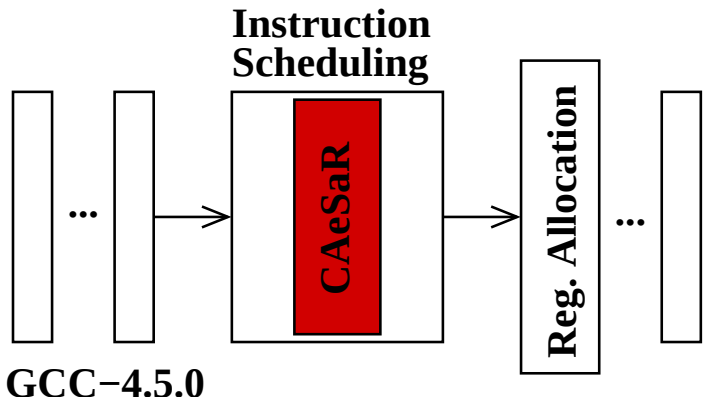


- Architecture
  - IA64-based 4 issue clustered VLIW
  - 2,4 clusters
  - 1 cycle Inter-Cluster Latency

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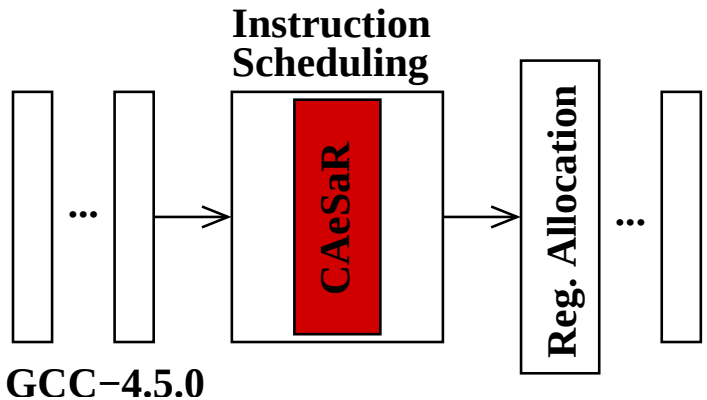


- Architecture
  - IA64-based 4 issue clustered VLIW
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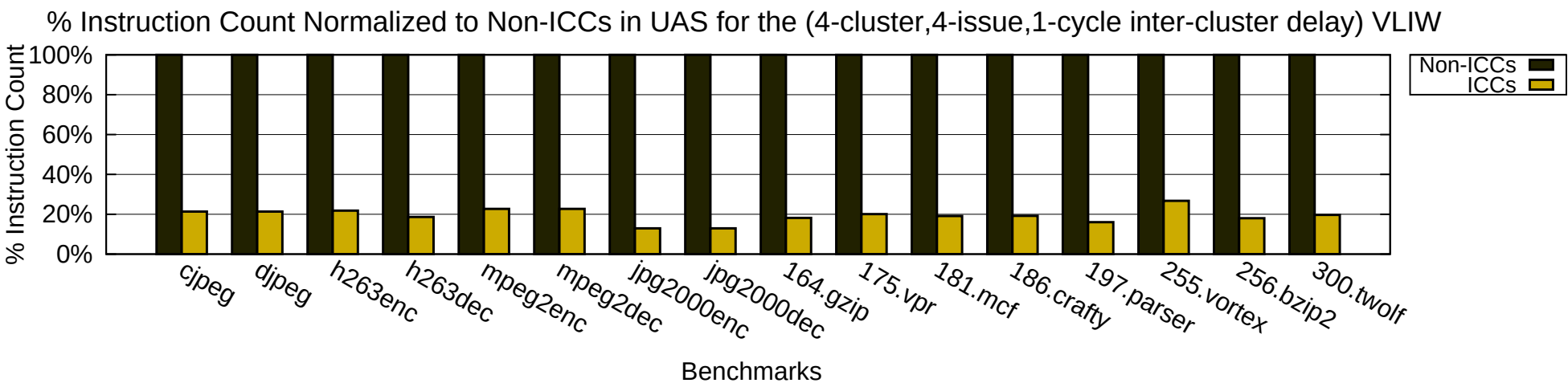
- Benchmarks: SPEC CINT2000 and MediabenchII Video

# Results: 4-cluster 4-issue, ICC ratio

- ICCs are a significant bottleneck



# Results: 4-cluster 4-issue, ICC ratio

- ICCs are a significant bottleneck
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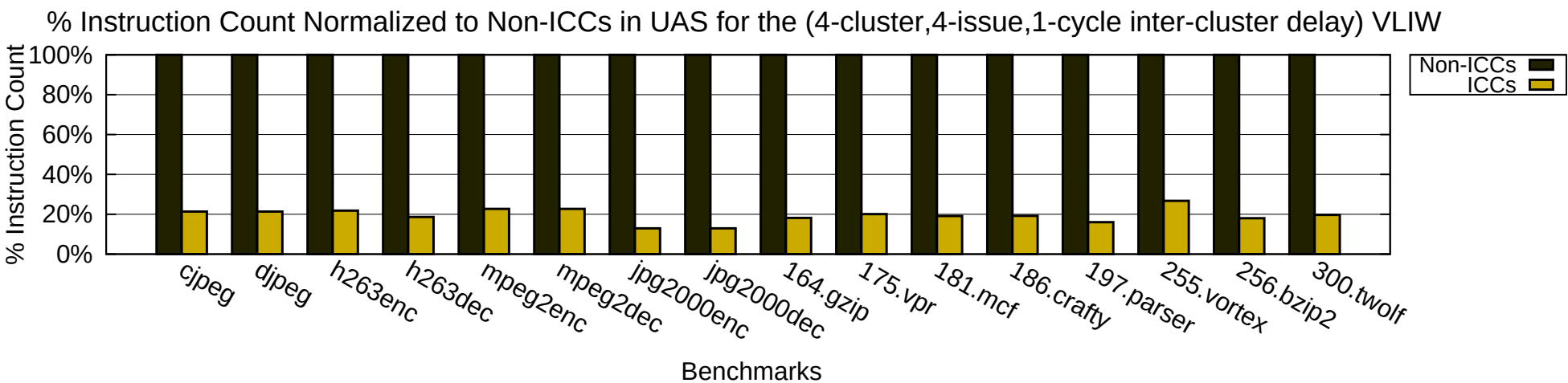

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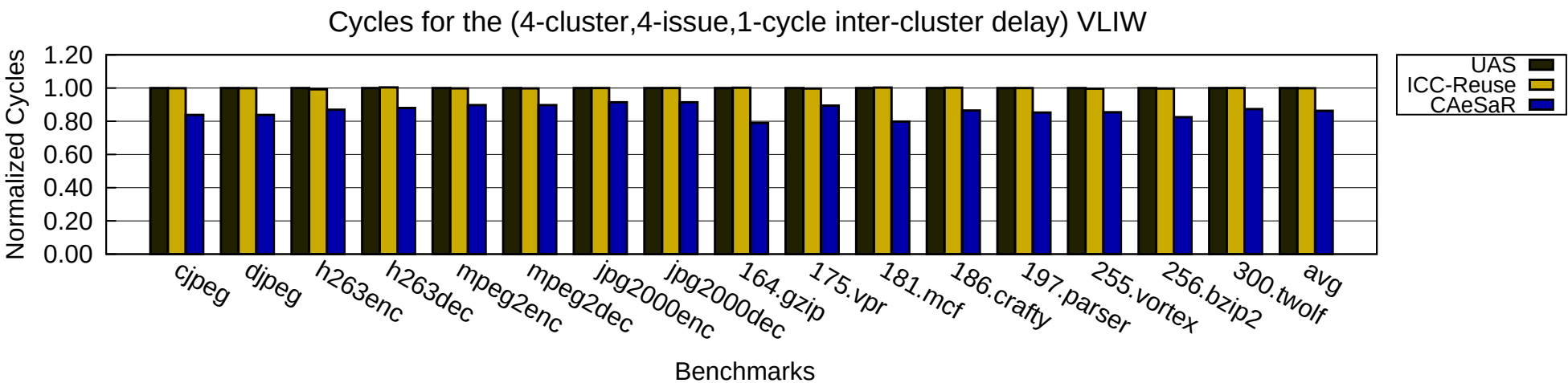

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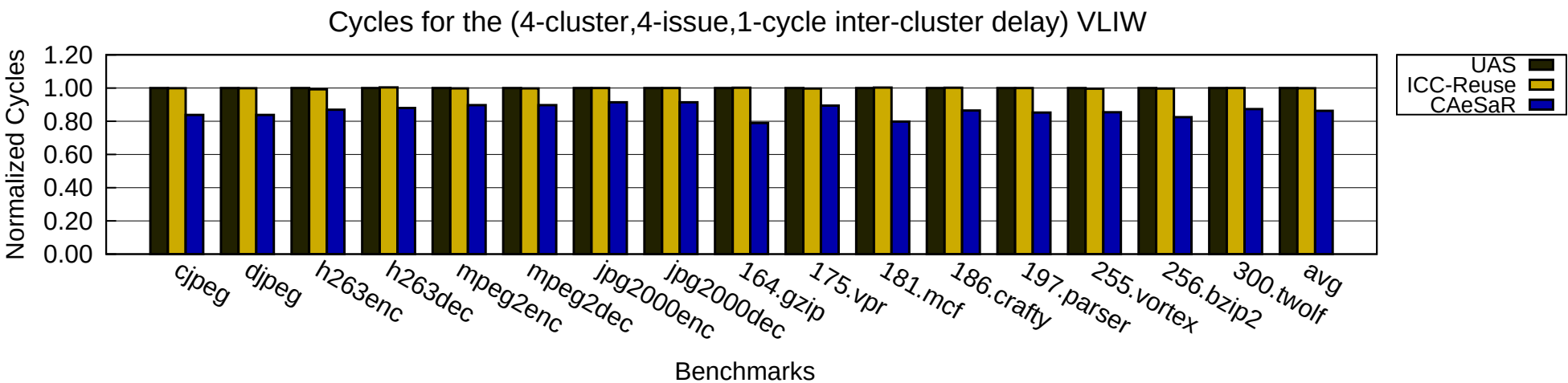

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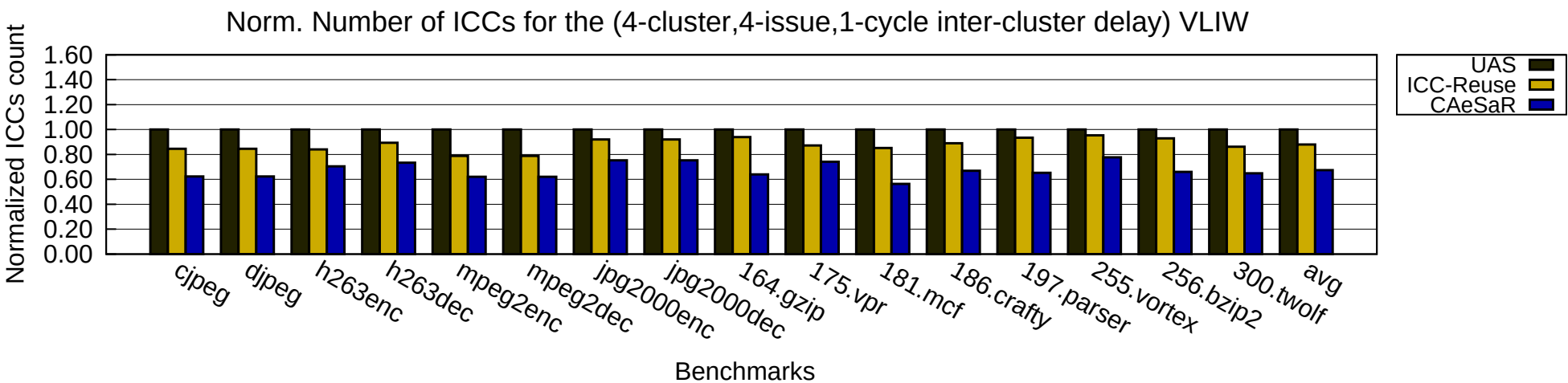

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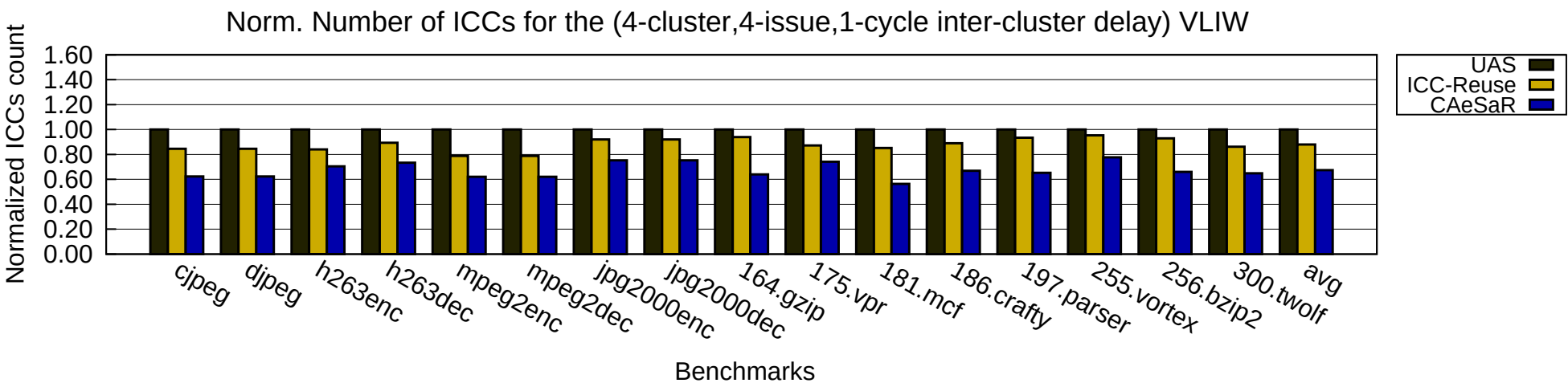
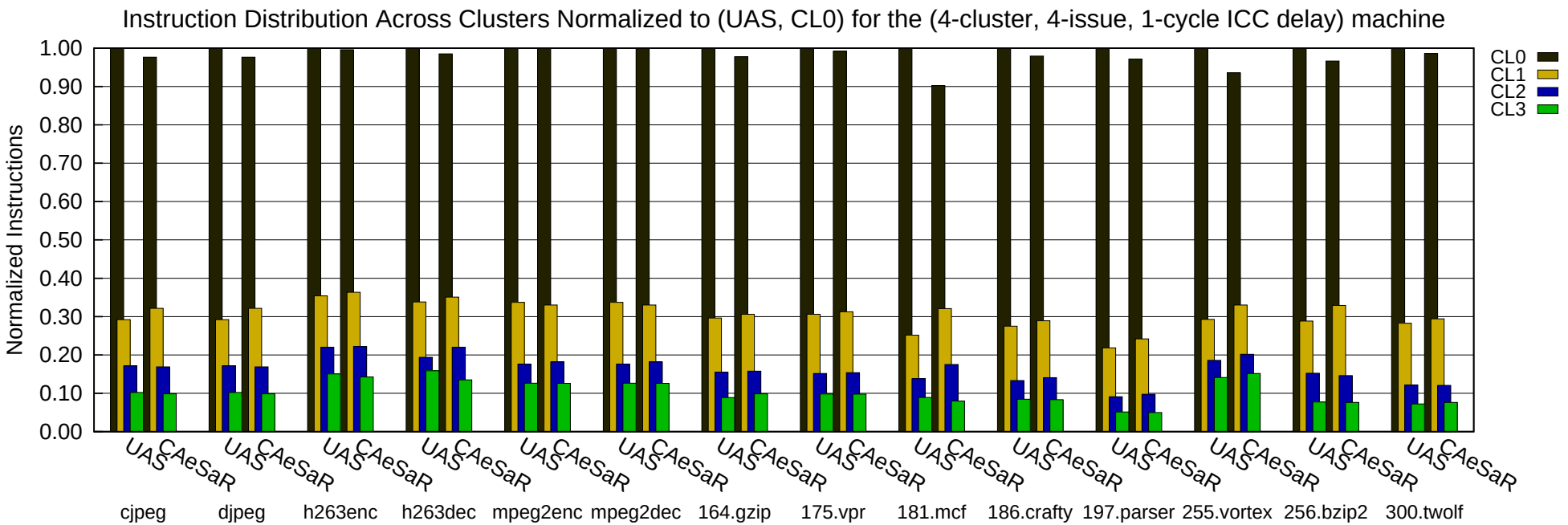


# Results: 4-cluster 4-issue, Instr Distribution

- Better resource utilization
- Less communication bottlenecks
- Potential for more ILP



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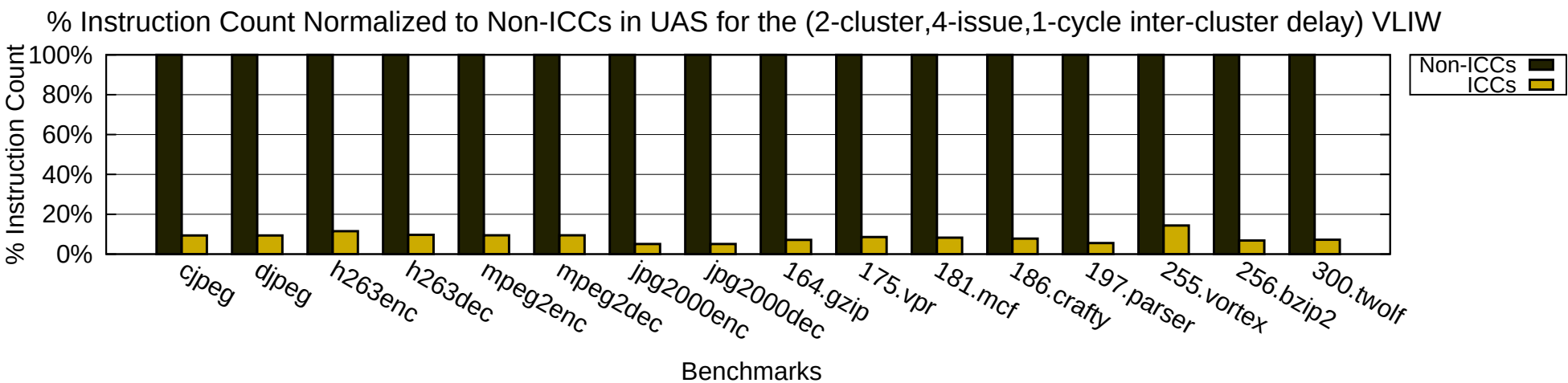

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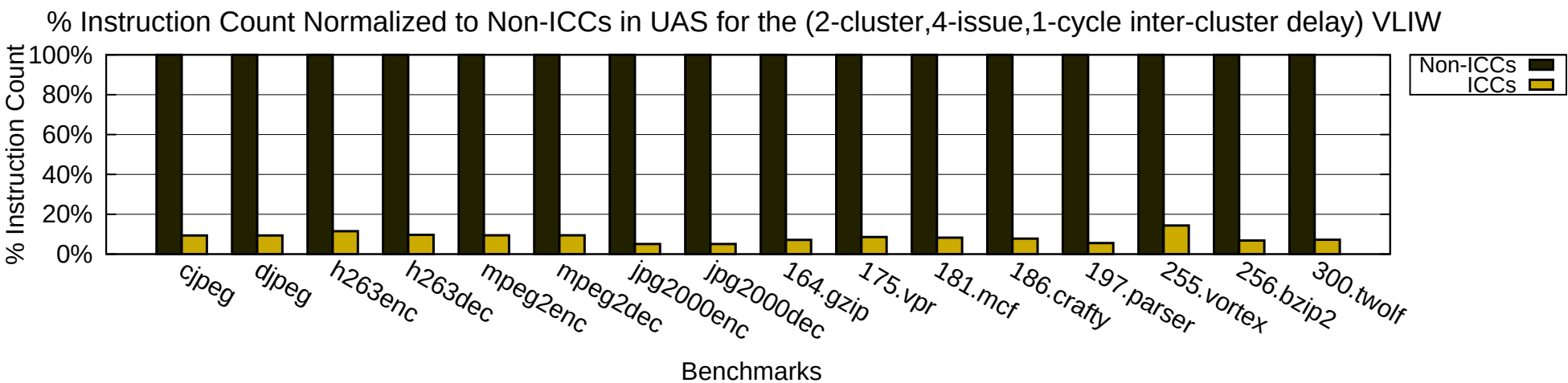

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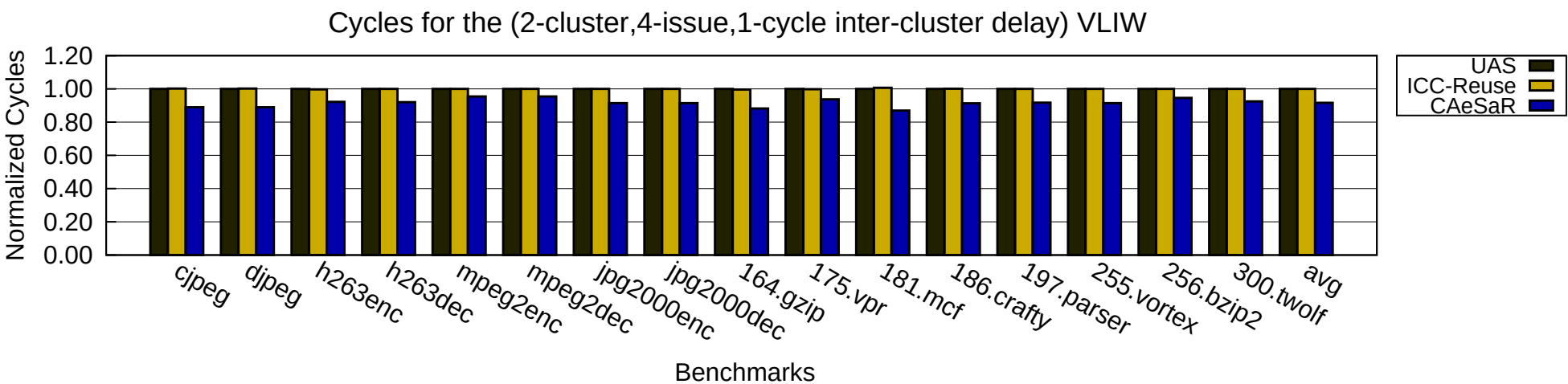

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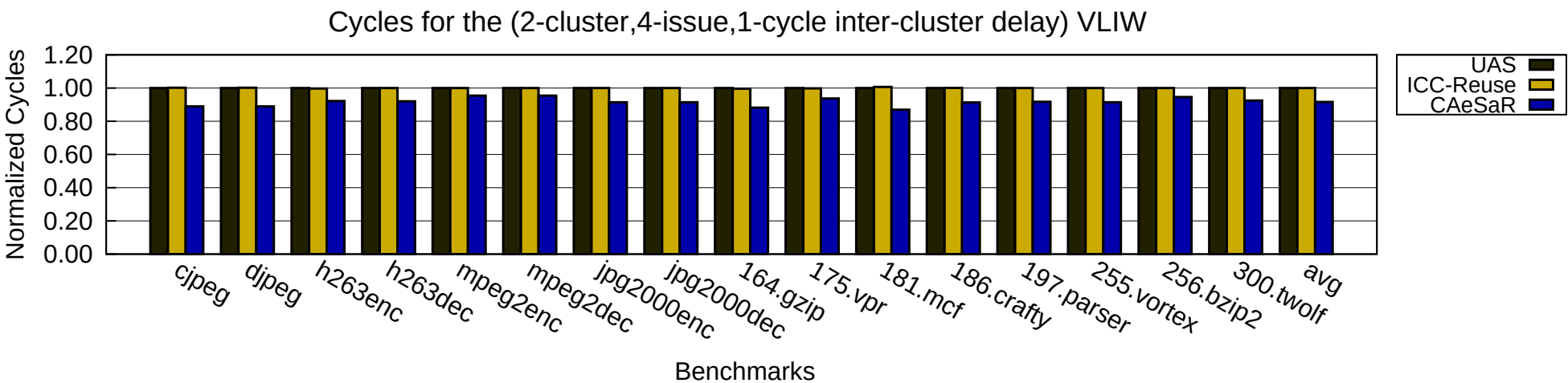

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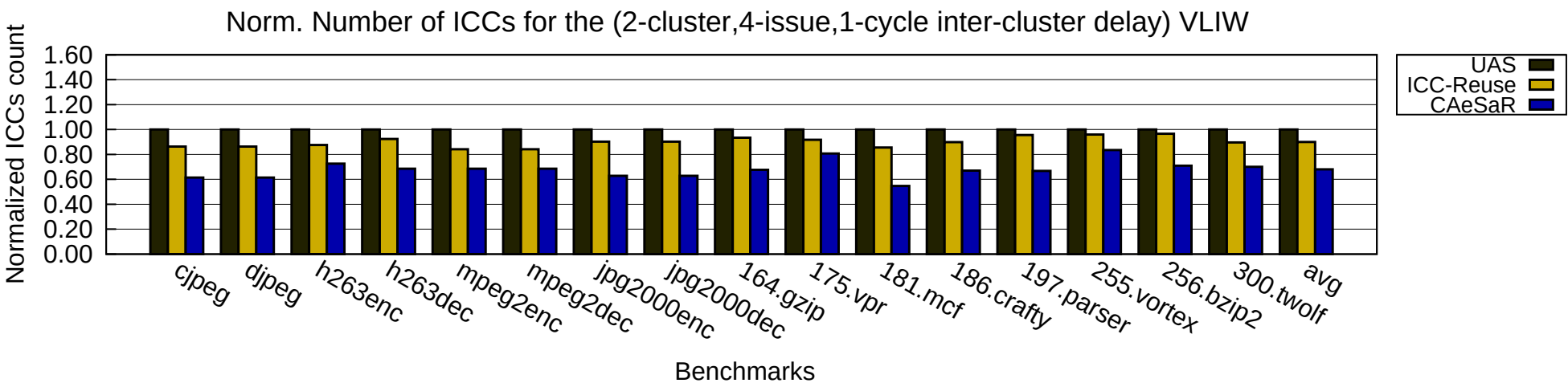

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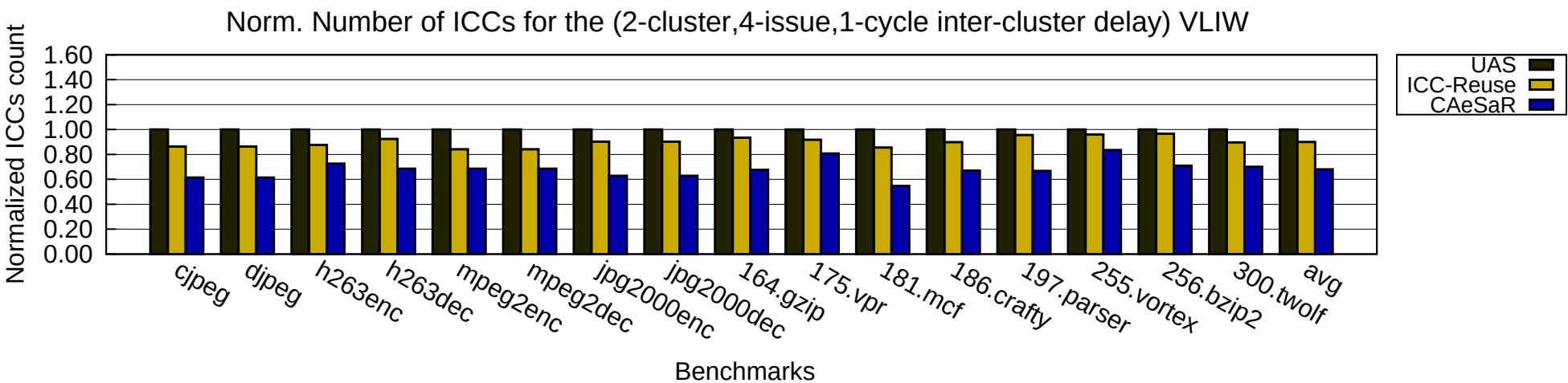

# Conclusion

Proposed CAeSaR Scheduling, a scheduler for clustered VLIWs that:

- Elliminates redundant Inter-Cluster copies
- Solves phase-ordering problem between Scheduling and ICC-reuse
- Generates more compact schedules compared to state-of-the-art

# CAeSaR: unified Cluster-Assignment Scheduling and communication Reuse for clustered VLIW processors

Vasileios Porpodas [†] and Marcelo Cintra [†⋆]

School of Informatics, University of Edinburgh[†]
Intel Labs Braunschweig[⋆]

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